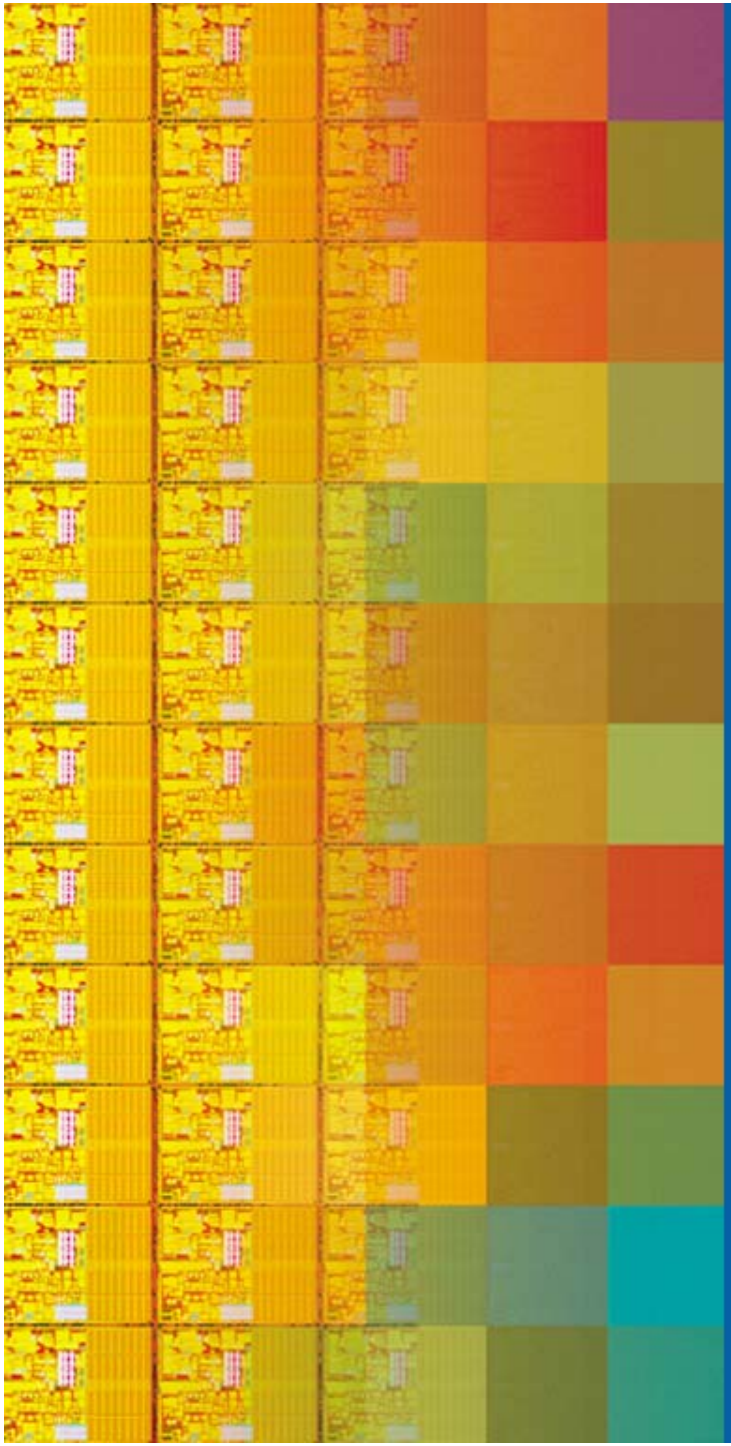

intel Leap ahead™

Intel Developer FORUM

Intel's Silicon R&D Pipeline

Paolo Gargini
Intel Fellow, Director of Technology Strategy
Technology & Manufacturing Group

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New Since IDF-Fall '05

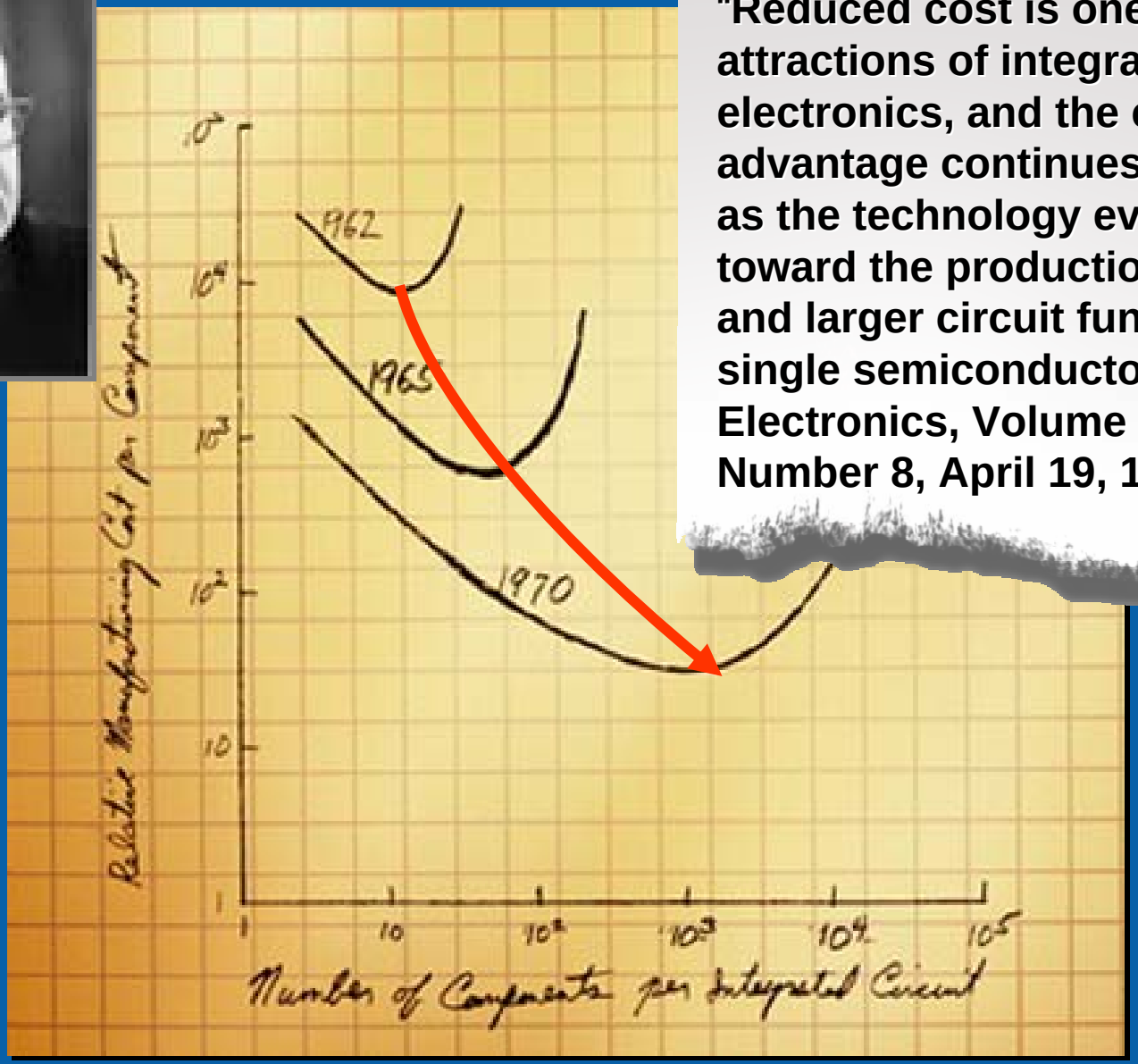
- Moore's Law
- Invest for the future
  - –65nm "ready"
  - –45nm "on time"
  - –R&D pipeline
- Support platforms
  - –Holistic approach
  - –Solid foundation

- No change
- From Intel only
  - –65nm products
  - –45nm SRAM
  - –InSb transistors
- >1 year ahead process
  - –65nm solutions
  - –Industry-leading low-leakage transistors

Key Messages

- Only Intel has the process technology pipeline
  - Follows Moore's Law on 2-year-cycle
  - 65nm production Q4'05: > 1-year-lead over competition
  - 45nm prototype Q1'06
  - 65nm/90nm cross-over Q3'06
  - Tech options '07 and beyond
- Process tech is an important competitive advantage for Intel platforms
  - Industry-leading low-leakage transistors provide a solid foundation
  - Holistic approach to world-class yield, energy-efficient performance, and leading-edge capacity

Gordon Moore, 1965



"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38, Number 8, April 19, 1965

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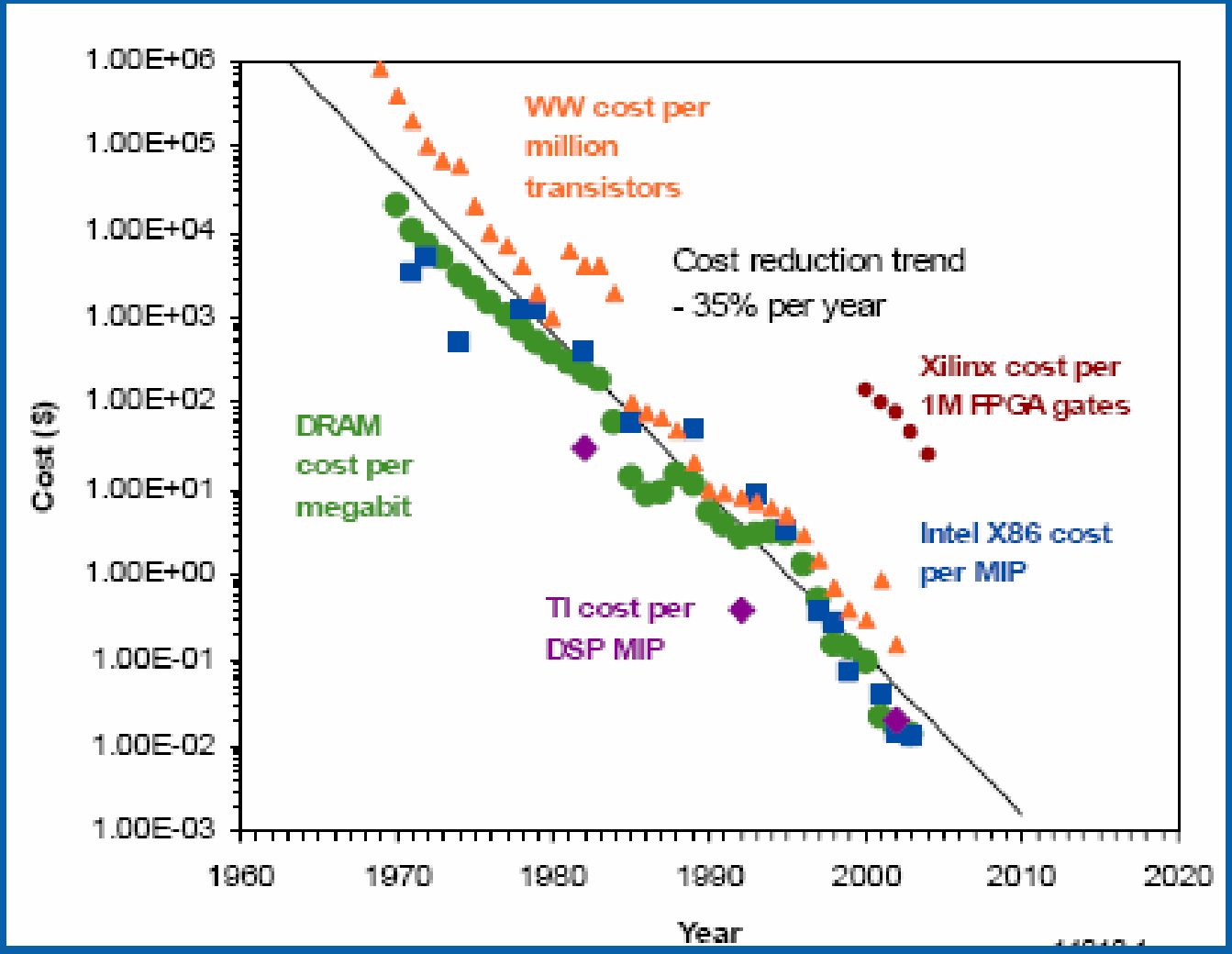
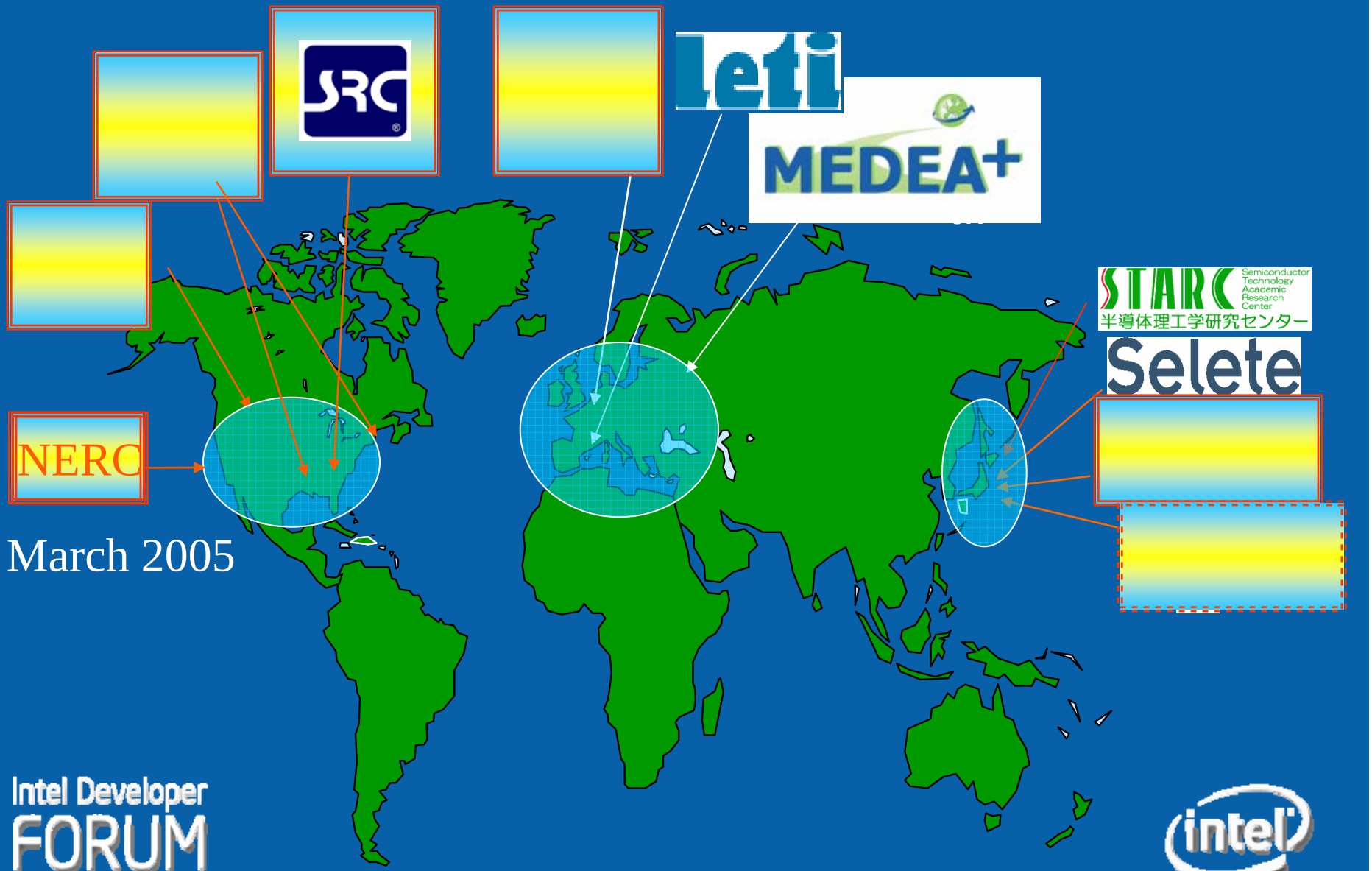
Moore's Law Delivers Value to the End User



With permission from
IC Knowledge LLC

Intel Consortia Research Landscape



March 2005

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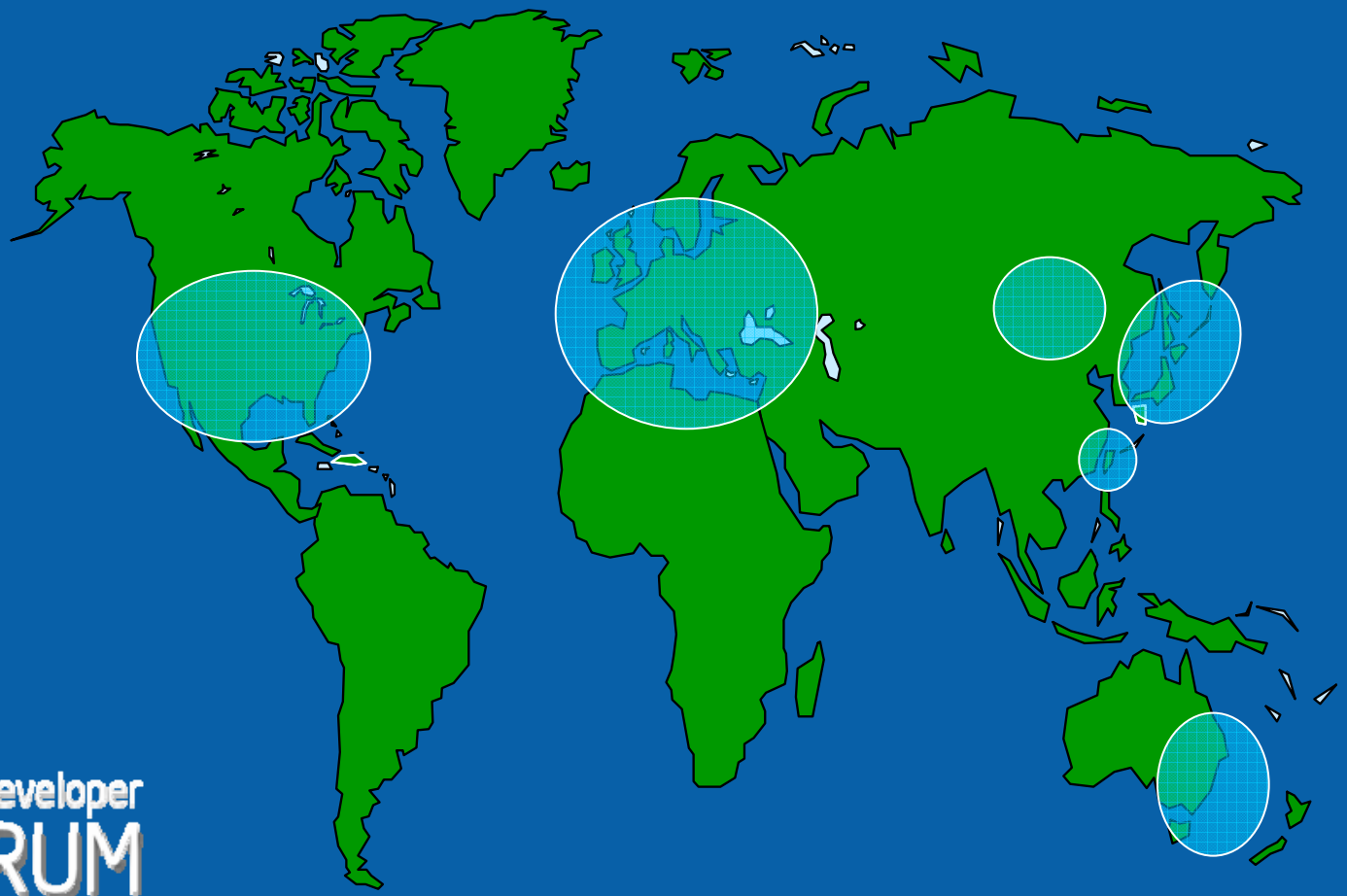
Intel University Research Landscape



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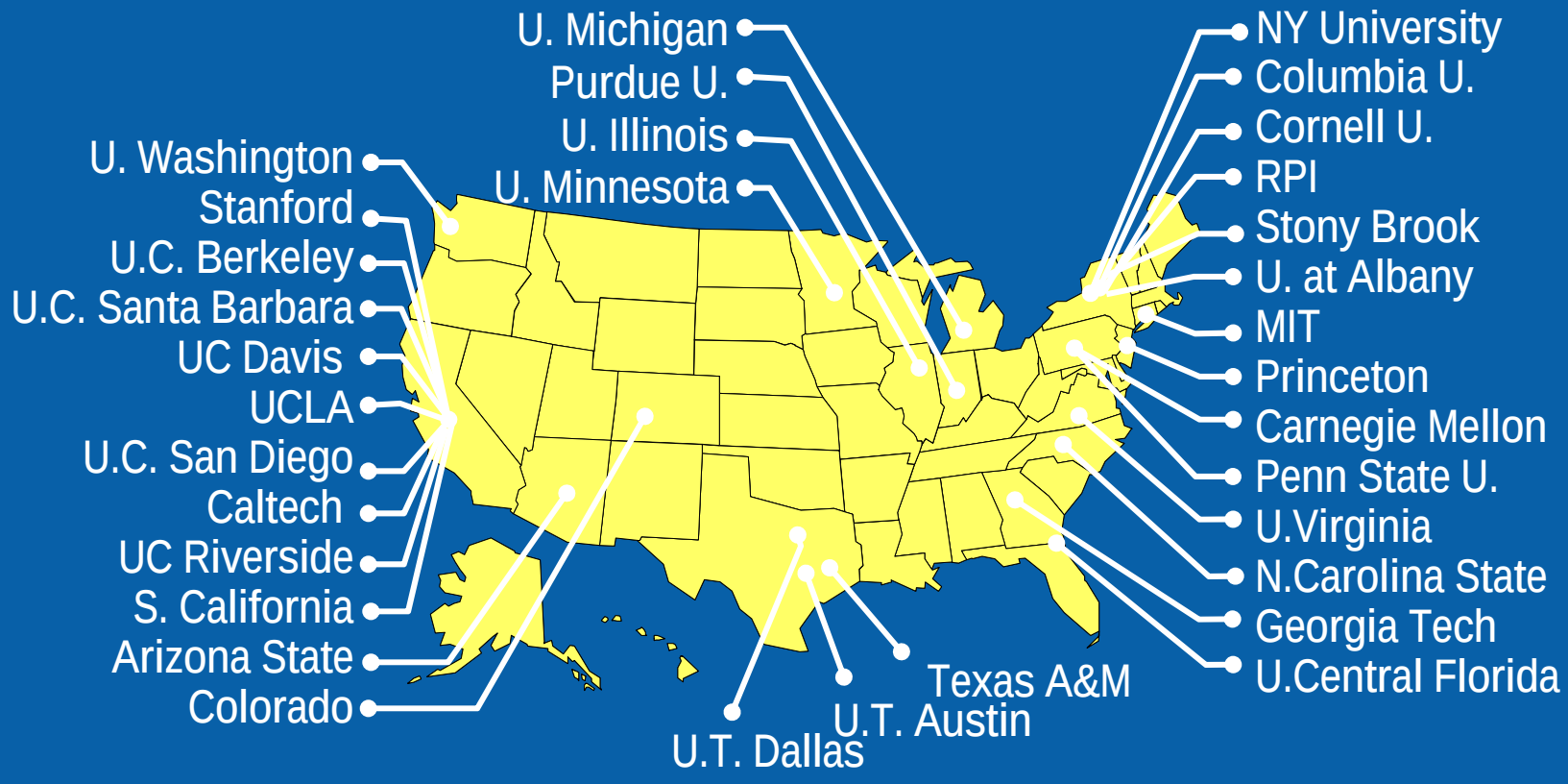
Intel University Research Network in the US



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Unwavering Commitment to Invest in R&D Pipeline

Nat'l Labs
Suppliers
Internal
Investment
University
Consortia

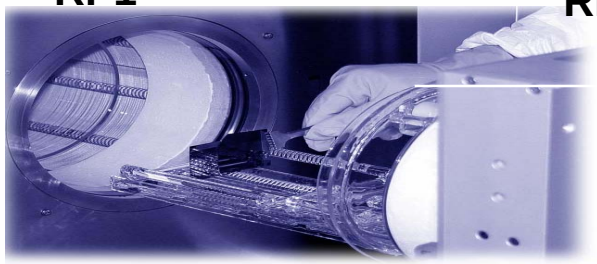
Extern Research

Materials
Equipment
Structures
Processes

Predevelopment

Development

Internal Research
RP1

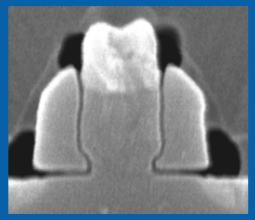
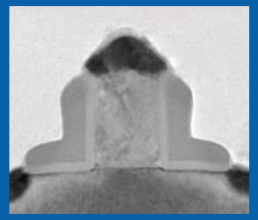
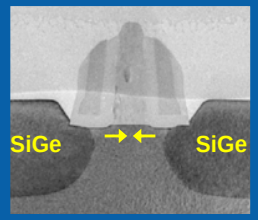
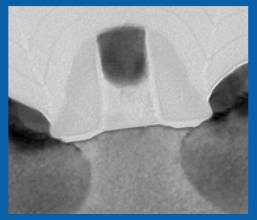
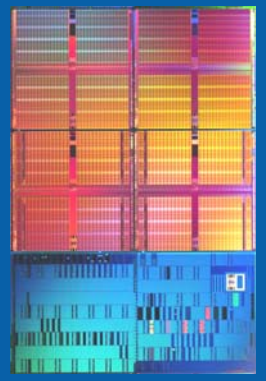
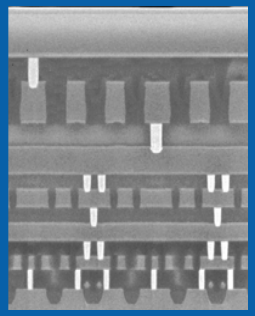
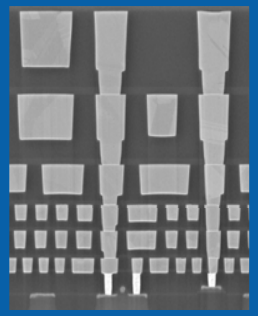
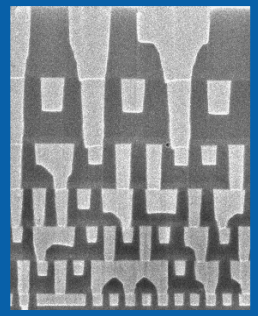
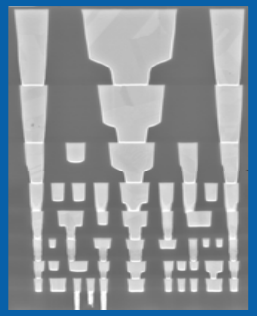


Pathfinding
RP1/D1D

Development
D1D

Manufacturing
D1D/Fabs

Intel only:
On-time “2-year-cycle”

	180nm	130nm	90nm	65nm	45nm
Wafer Size (mm):	200	200/300	300	300	300
1st Production:	1999	2001	2003	2005	2007
Transistors:					
Interconnects:					
	100nm L_G $CoSi_2$ 6 Al SiOF	**70nm L_G $CoSi_2$ 6 Cu SiOF**	**50nm L_G NiSi Strain Si 7 Cu Low-k**	**35nm L_G NiSi Strain Si 8 Cu Low-k**	**Details Coming!**

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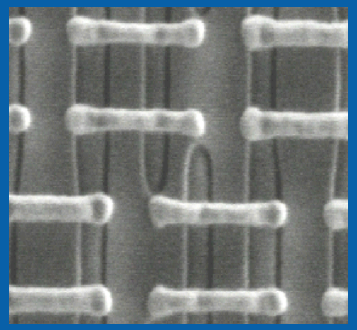
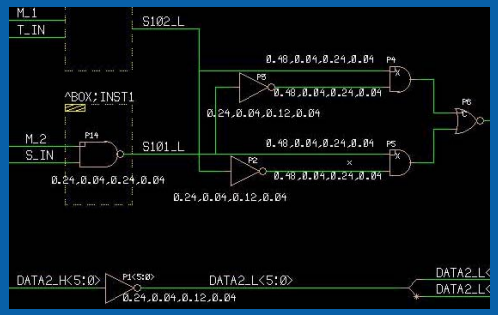
Intel only:
In-house co-optimization

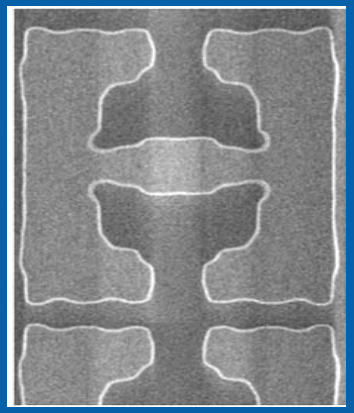


Process

Leading-edge capacity



Design



Masks

Packaging

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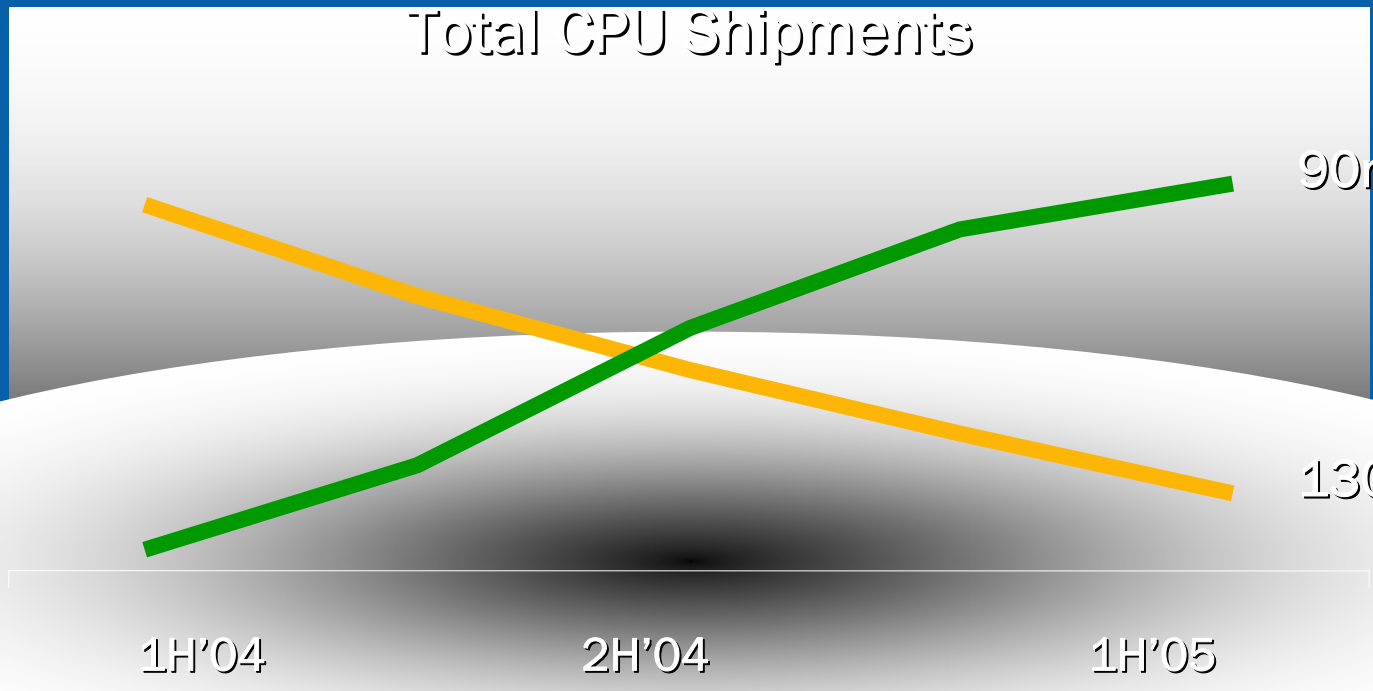
Intel Ahead of Industry on 90nm Ramp



130nm to 90nm crossover 3Q'04

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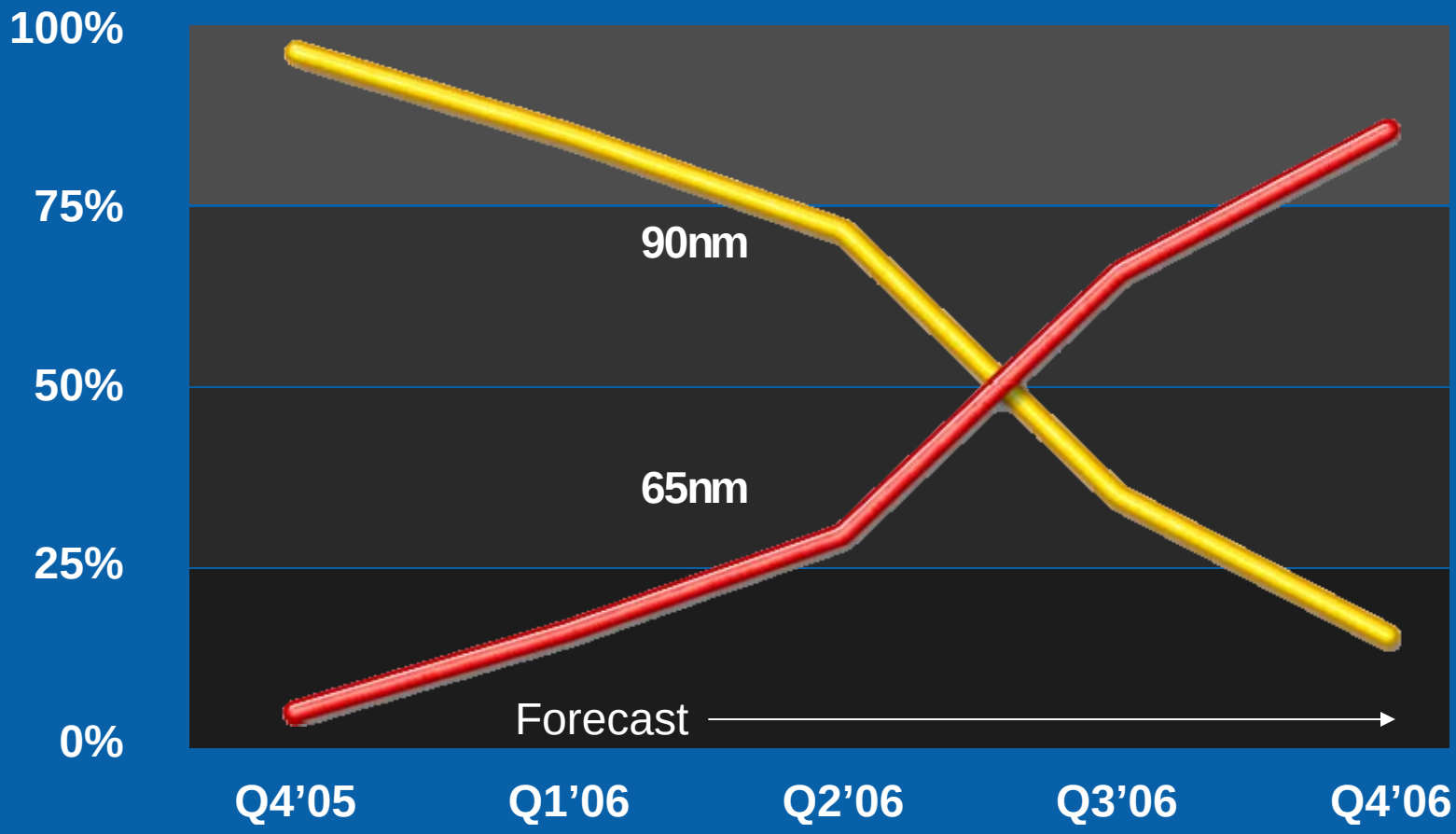
Only from Intel: 65 nm process / products / production



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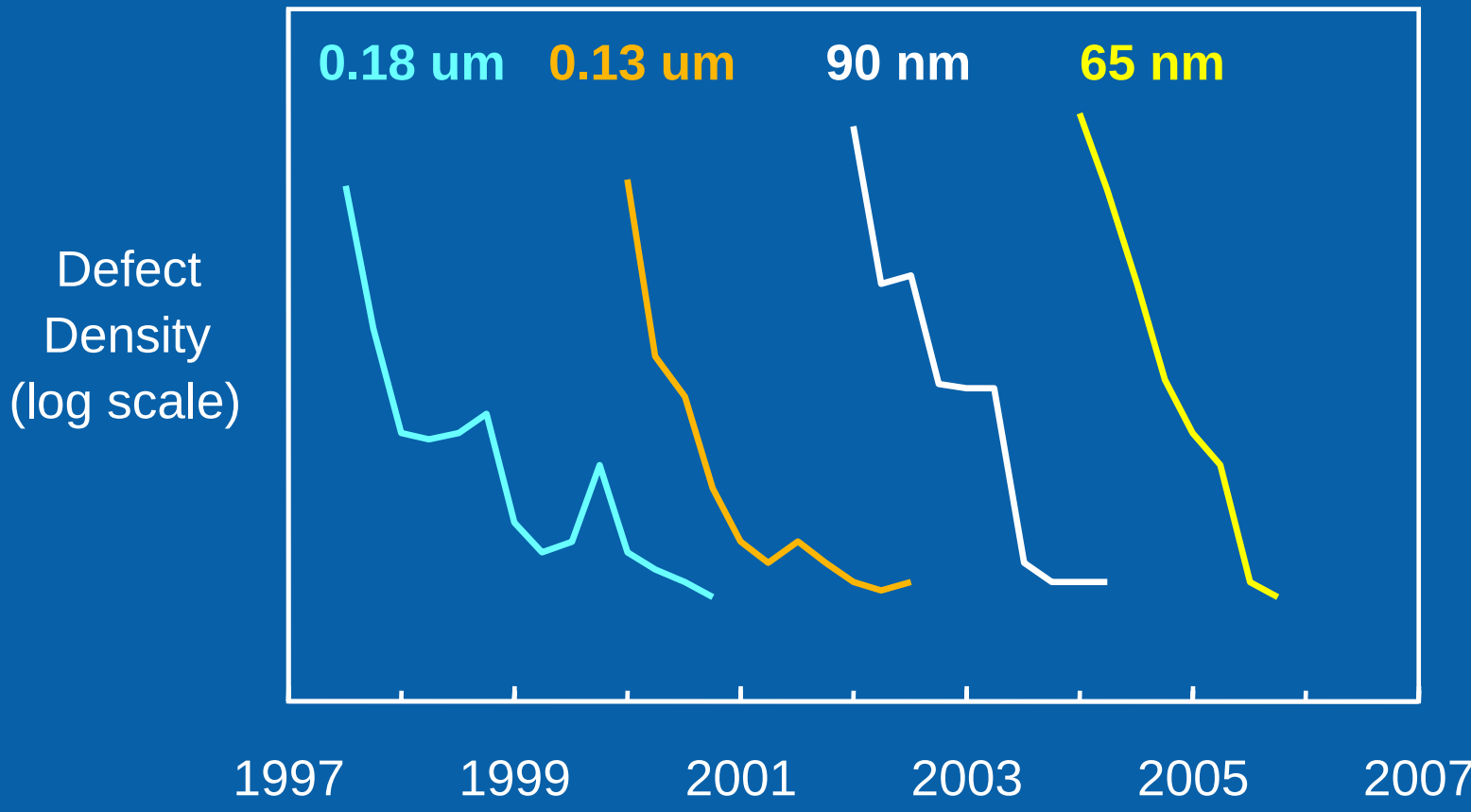
Crossover projected for Q3'06

intel

Intel Only: Predictable World-Class Yield on 2 Year Cycles



***Copy Exactly*! transfer methodology enables matched yield at new factory startup**

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Moore's Law in Action: Microprocessors Advance

1.0µm 0.8µm 0.6µm 0.35µm 0.25µm 0.18µm 0.13µm 90nm 65nm

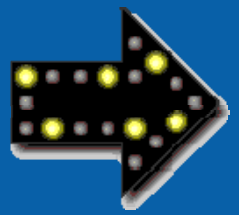
Intel 486™ Processor

Pentium® Processor

Pentium® II/III Processor

Pentium® 4 Processor

Intel® Core™ Duo Processor



Source: Intel

Intel only: Economy of scale enables in-house co-optimization

Ronler Acres, Oregon

300mm research, development, and production on one campus

Power Challenges Are Neither New Nor Fundamental

"Will it be possible to remove the heat generated by 10's of thousands of components?"

G. Moore, *Cramming more components onto integrated circuits*, Electronics, Volume 38, Number 8, April 19, **1965**

Intel Leads Transition from Classical Scaling to Power-Efficient Scaling

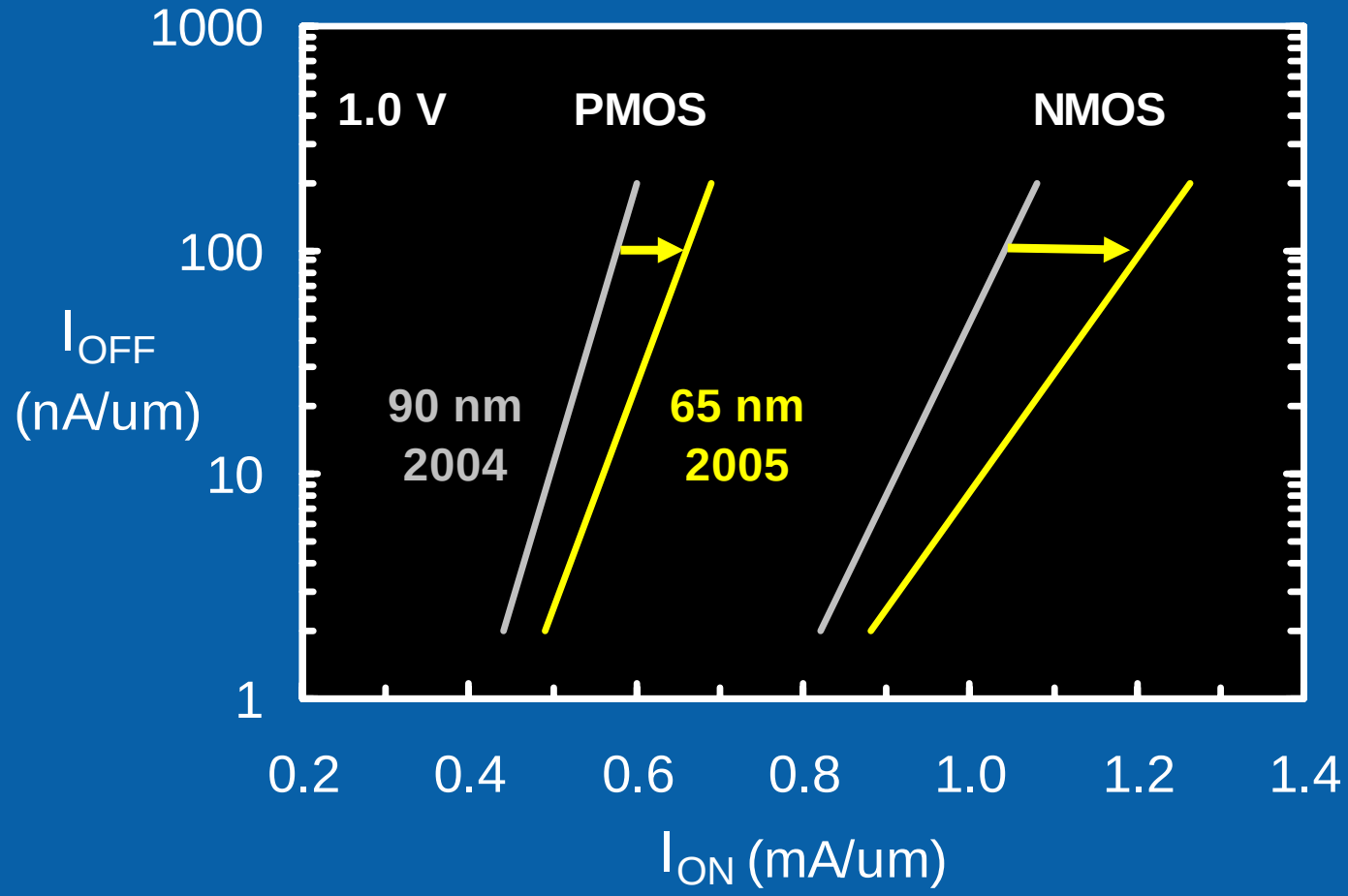
1970's: Classical/Constant-Vdd -> PMOS, NMOS

1980's: Classical/Constant Vdd -> CMOS

1990's: Classical/Voltage scaling -> ($P = CV^2f$)

2000's: Power-efficient scaling -> New processes, materials, structures; co-optimization with design

Increased Transistor Performance With 2nd Generation Strained Silicon



~16% higher drive current plus ~20% lower gate capacitance improves transistor switching speed by >20% at same leakage level

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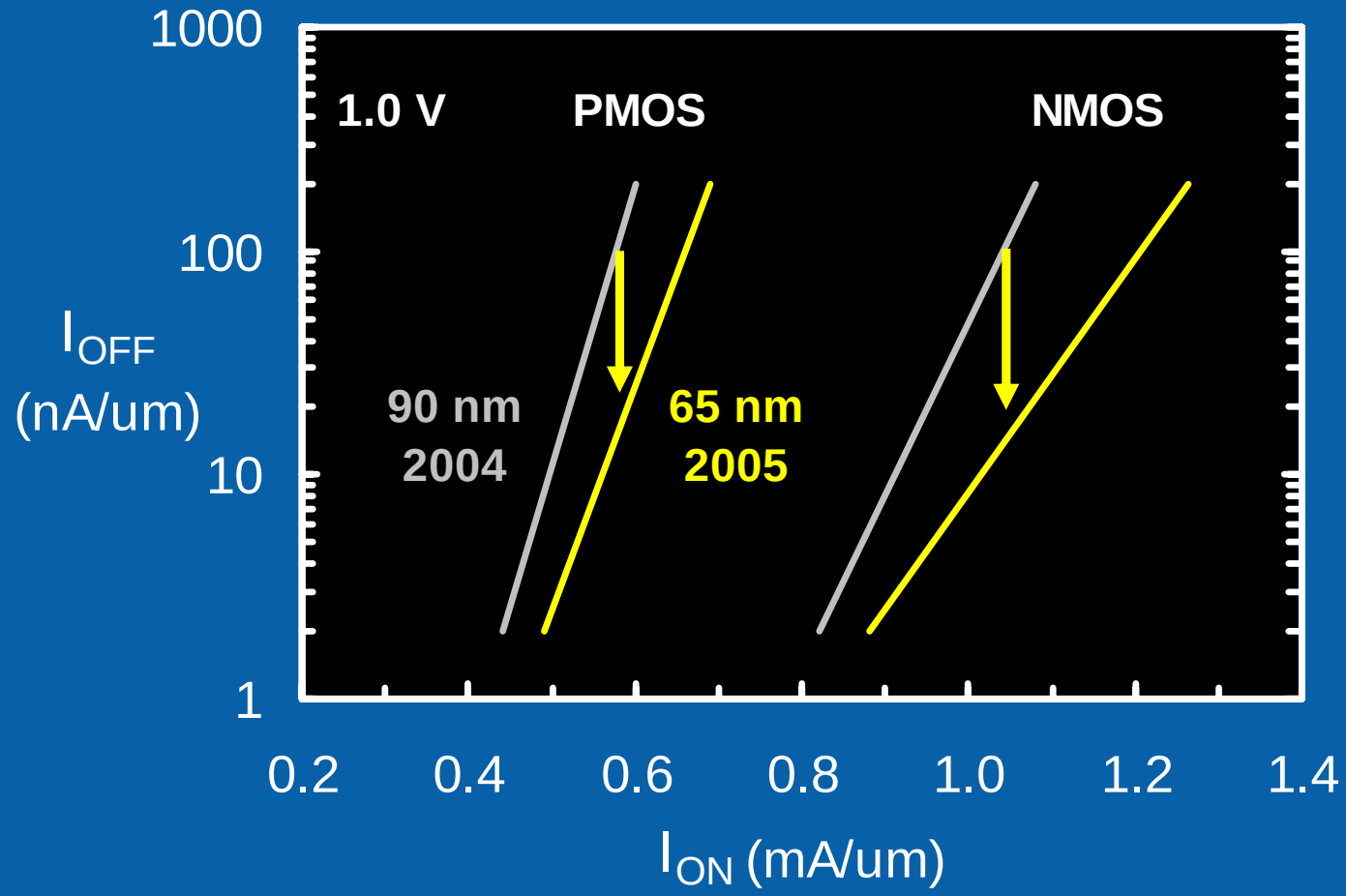
Reduced Transistor Leakage With 2nd Generation Strained Silicon



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Or, transistor leakage can be reduced ~5x at same drive current

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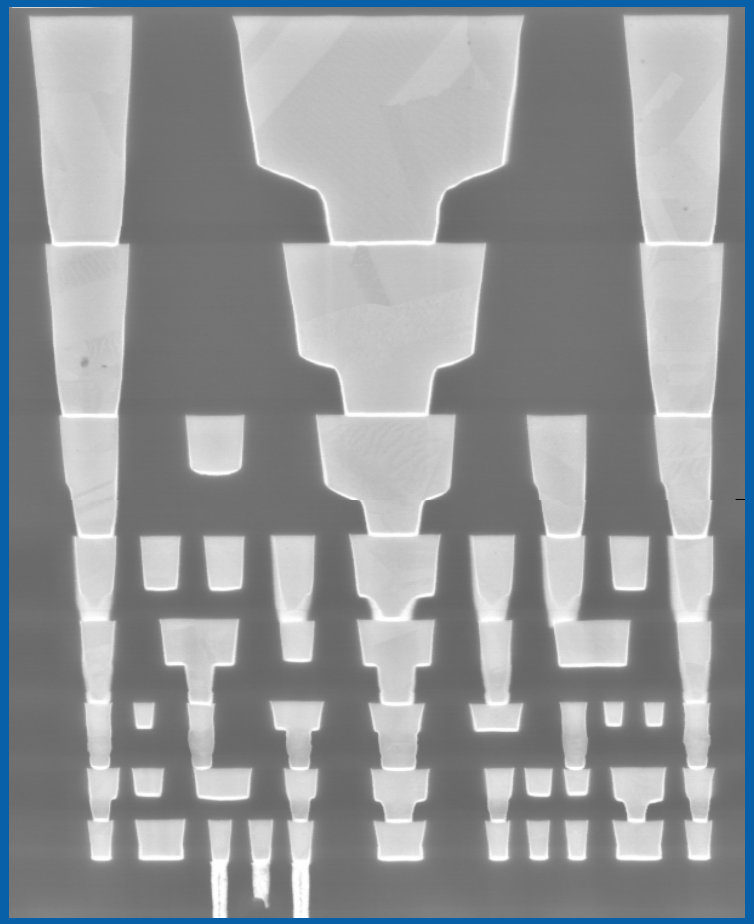
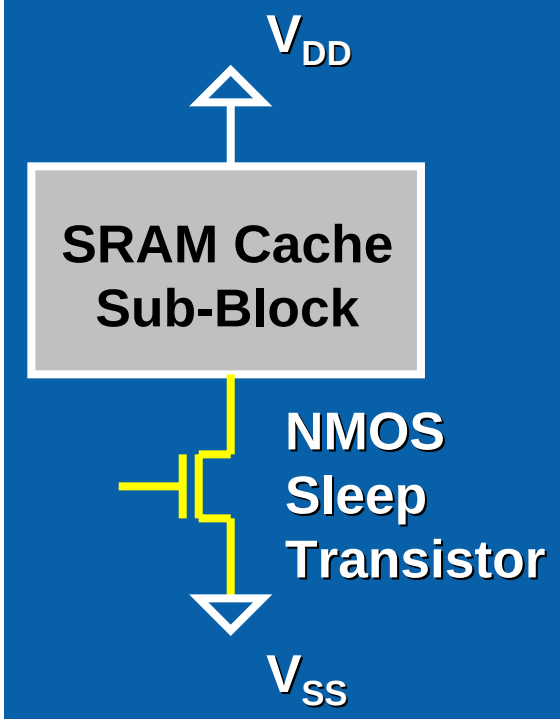
Power Efficient Interconnect Includes 2nd Generation CDO

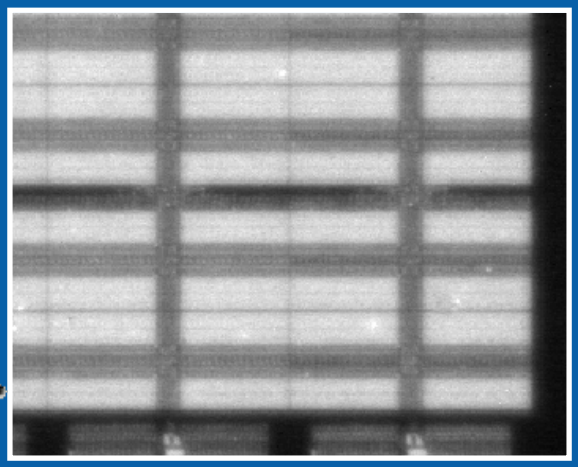
- Low-k carbon doped oxide (CDO) dielectric reduces interconnect capacitance (improved from 90 nm generation)
- Metal 8 layer is added for improved density and performance (1 more layer than 90 nm generation)
- Interconnect capacitance is reduced by use of low-k dielectric and by ~0.7x line length scaling
- Lower capacitance improves interconnect performance and reduces chip power

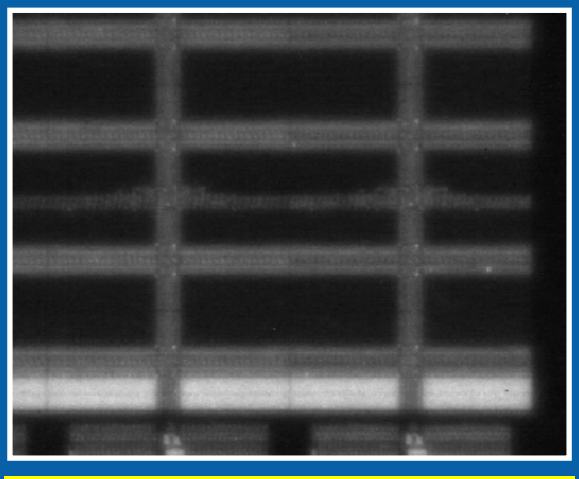


Sleep Transistors Reduce Leakage Power



70 Mbit SRAM IR photos



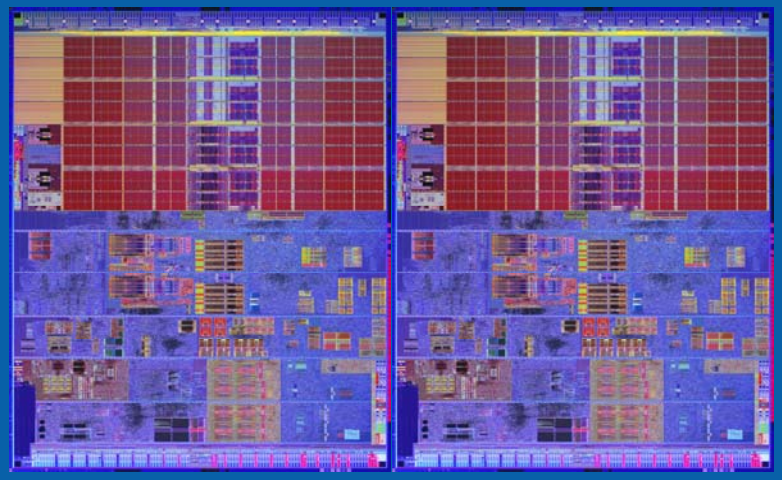


Normal SRAM sub-block leakage

Sleep transistors shut off leakage in inactive sub-blocks

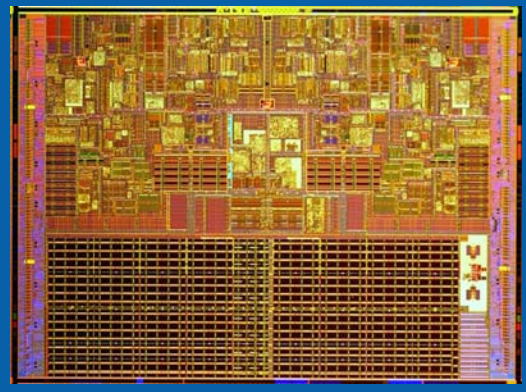
>3x SRAM leakage reduction with use of sleep transistors

Dual Core on 65 nm



Intel® Pentium® Processor
Extreme Edition 955

162 mm²
376M transistors



Intel® Core™ Duo Processor

90 mm²
151M transistors

Intel shipped millions of dual core CPUs in 2005 and expects to ship >60 million multi-core processors by end of 2006

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65 nm Status Summary

- Nobody but Intel shipping 65nm since Oct. 2005
- Only Intel has two 65nm/300mm fabs shipping in volume (D1D and Fab 12); with two more coming in 2006
- Intel has shipped more than a million dual-core processors made on 65nm process technology
- Intel has shipped hundreds of million of Strained Silicon CPU's

45 nm Logic Process on Track for Delivery in 2007

Process Name	P1262	P1264	P1266	P1268
Lithography	90 nm	65 nm	45 nm	32 nm
1st Production	2003	2005	2007	2009

Moore's Law continues!

Intel continues to develop a new technology generation every 2 years

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45 nm Technology Benefits

Compared to today's 65 nm technology, the 45 nm technology will provide the following product benefits:

- ~2x improvement in transistor density, for either smaller chip size or increased transistor count
- >20% improvement in transistor switching speed or >5x reduction in leakage power
- >30% reduction in transistor switching power

This process technology will provide the foundation to deliver improved performance/Watt that will enhance the user experience

45 nm SRAM Chip

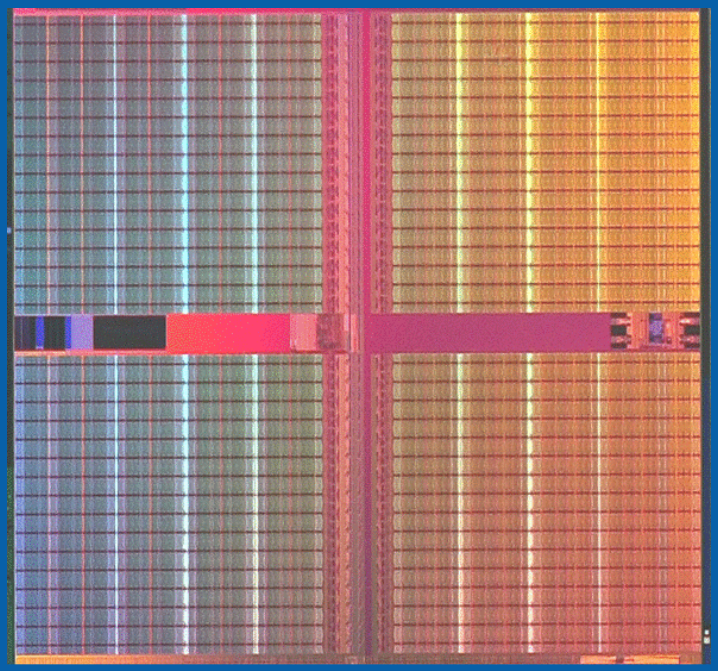
0.346 μm^2 cell

153 Mbit density

119 mm^2 chip size

>1 billion transistors

Functional silicon in Jan '06



45 nm SRAM test vehicle includes all transistor and interconnect features to be used on 45 nm microprocessor

No other company is capable of making a 45nm SRAM with the density and features we have until 2007 or later

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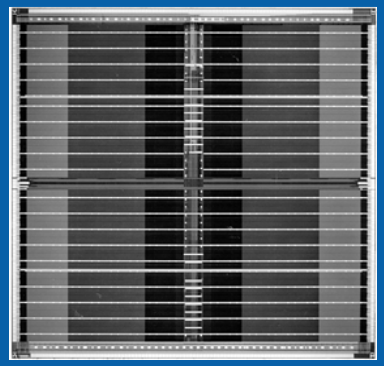
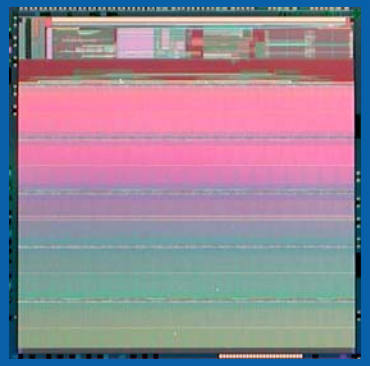
Intel SRAM Test Chips



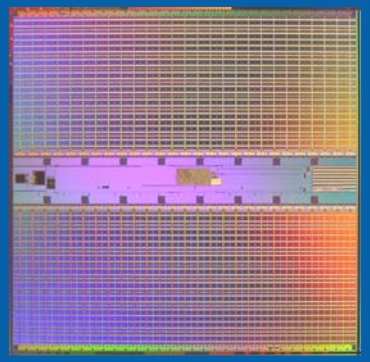
130 nm Process

2.45 μm² cell
18 Mbit
103 mm²
March ‘00



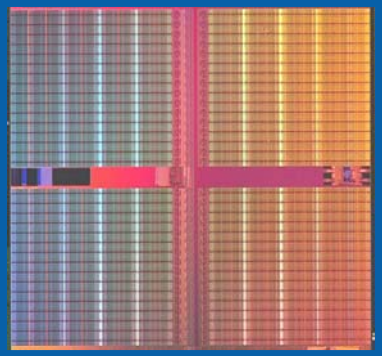
90 nm Process

1.0 μm² cell
50 Mbit
109 mm²
February ‘02



65 nm Process

0.57 μm² cell
70 Mbit
110 mm²
April ‘04



45 nm Process

0.346 μm² cell
153 Mbit
119 mm²
January ‘06

New SRAM test vehicle developed every 2 years to lead development of logic technologies

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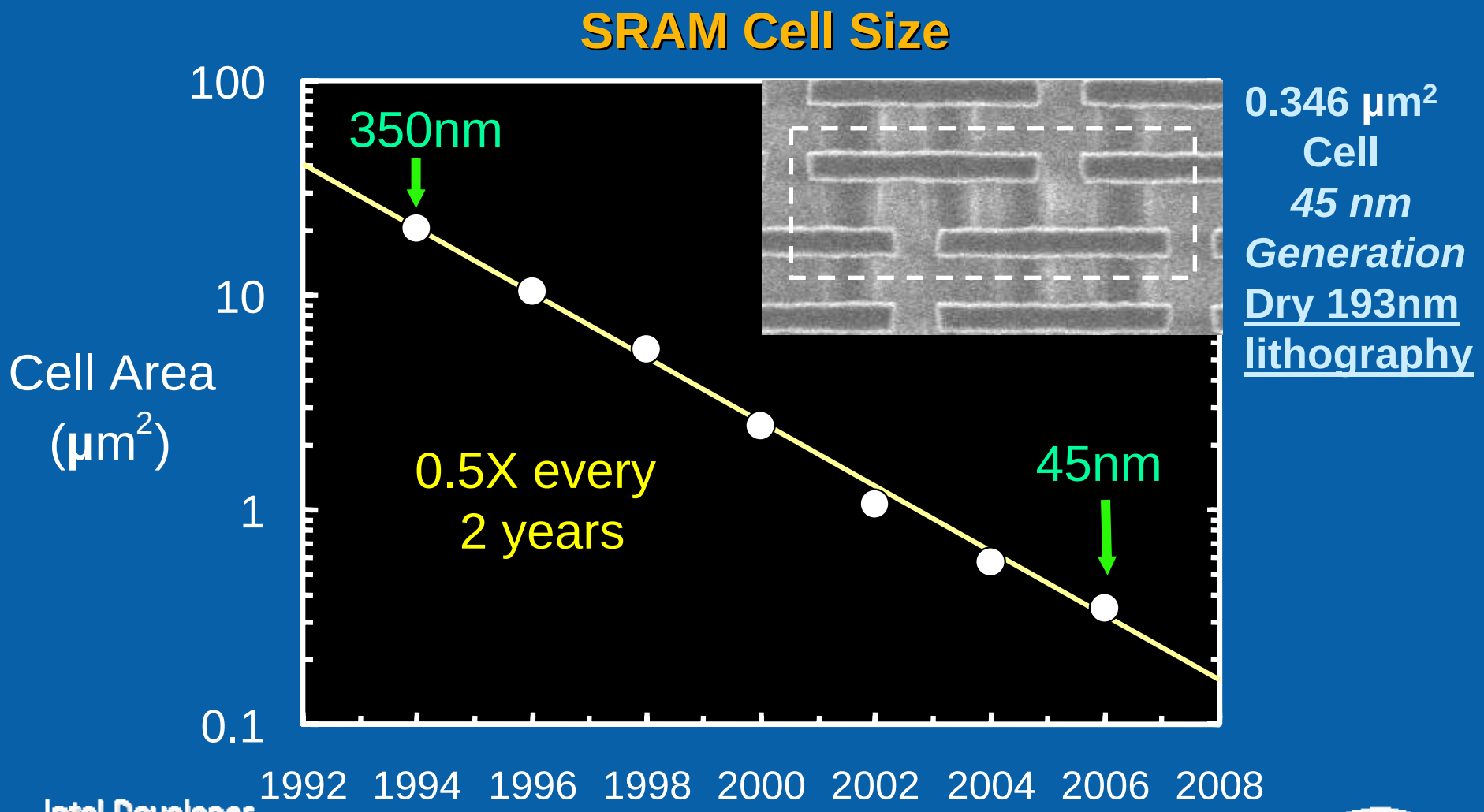
Intel's Density Scaling on Track



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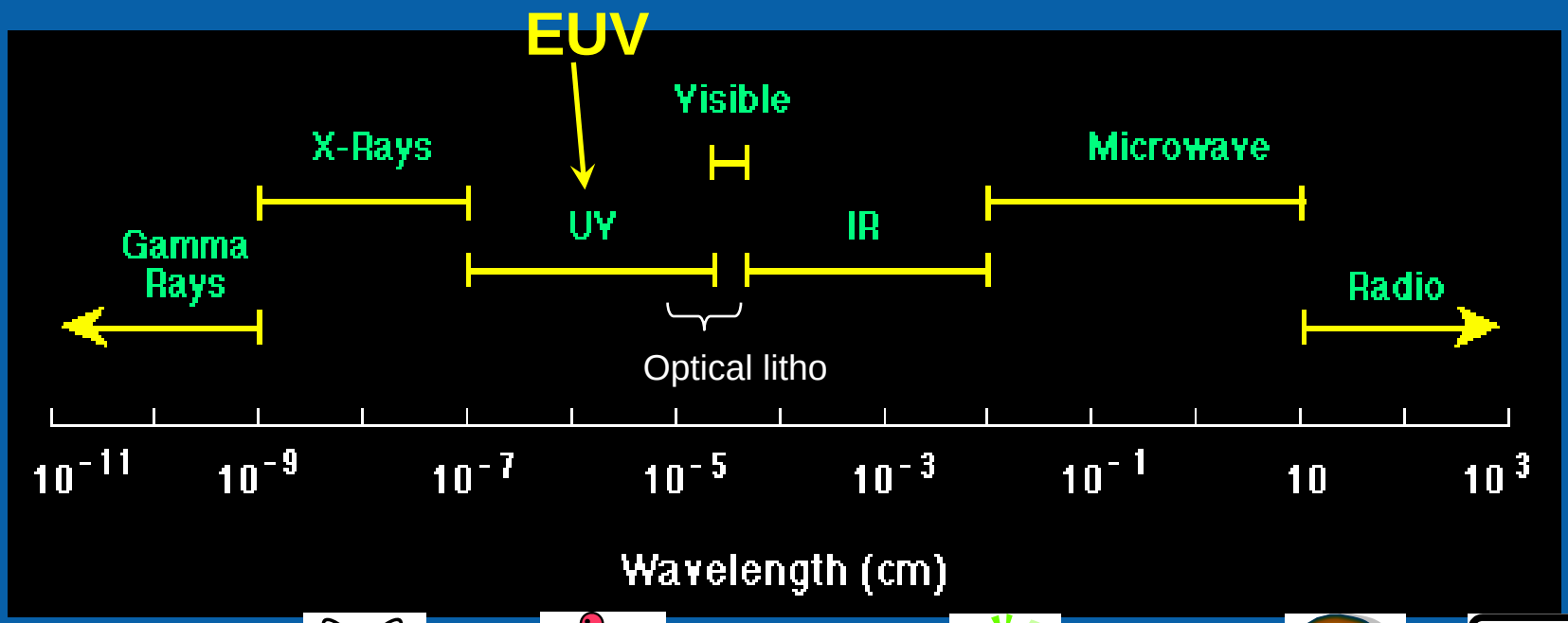
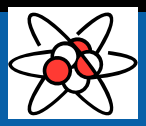
We Continue to Make Progress on EUV Lithography

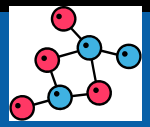
Power source

Mask defects

EUV pellicles




atom

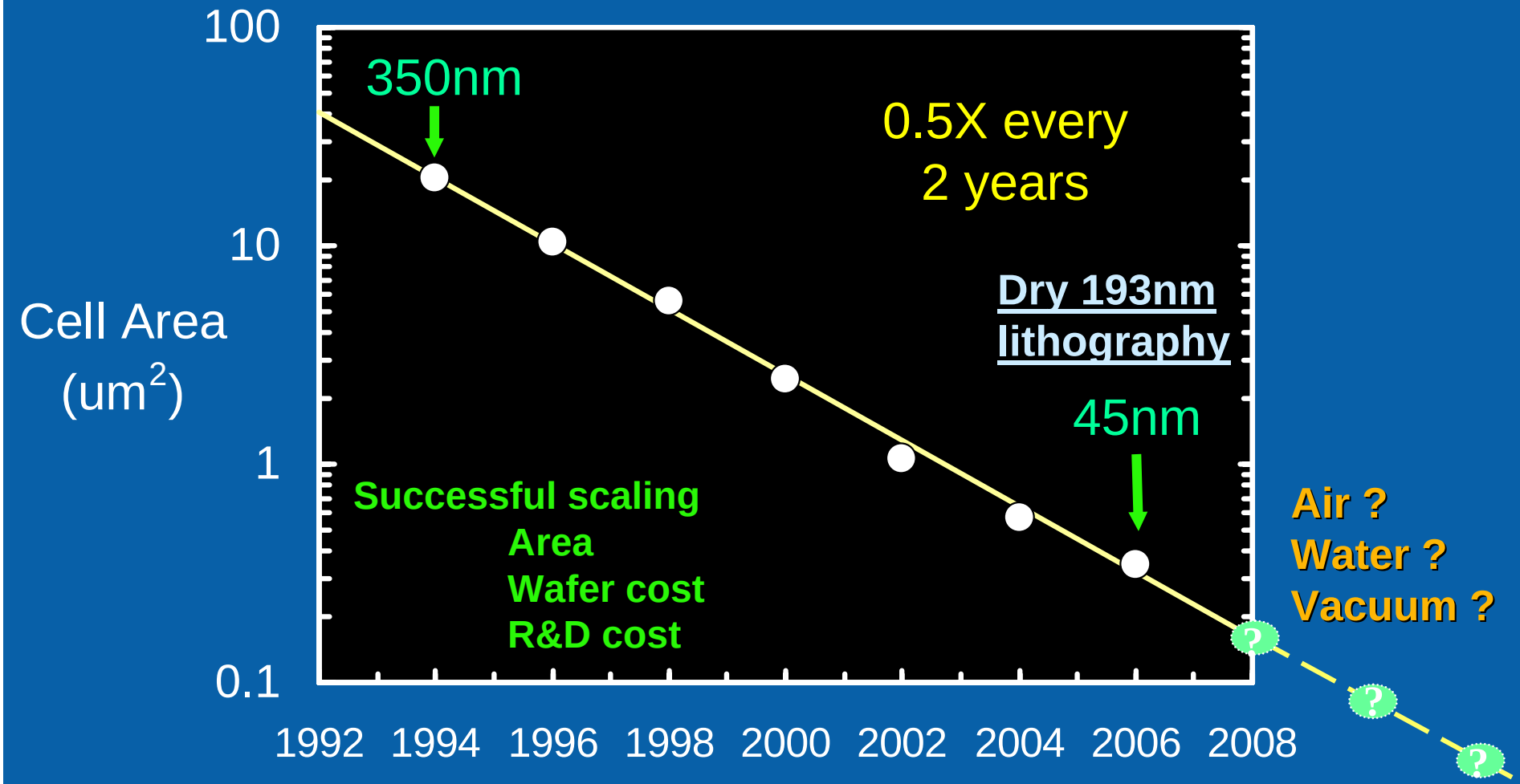

molecule


thickness of a dollar bill


softball


house

32nm Can be Done Without EUV (Choices are good!)



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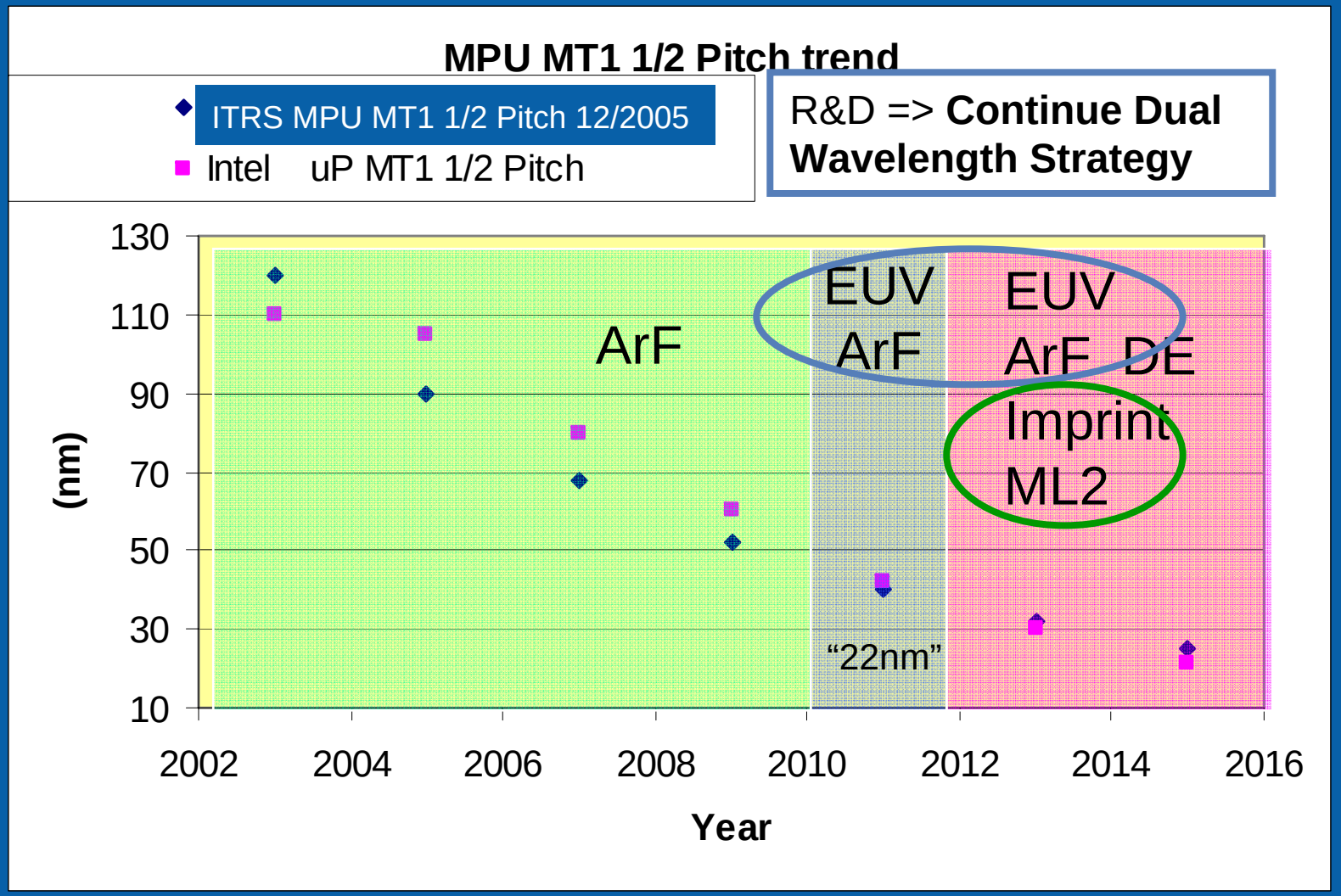
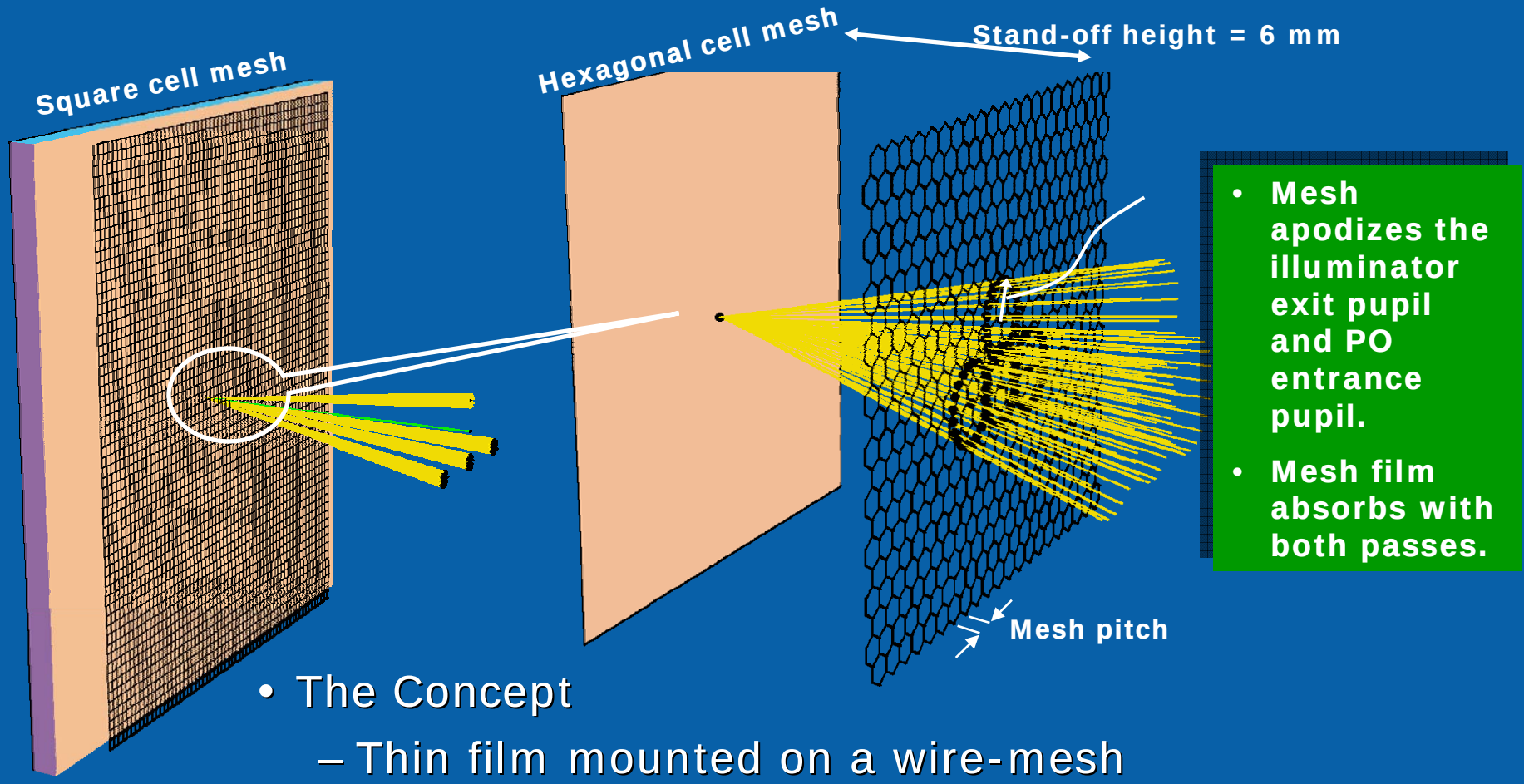
Multiple Litho Choices for 2011 – 2015

Continue Dual Wavelength R&D Strategy



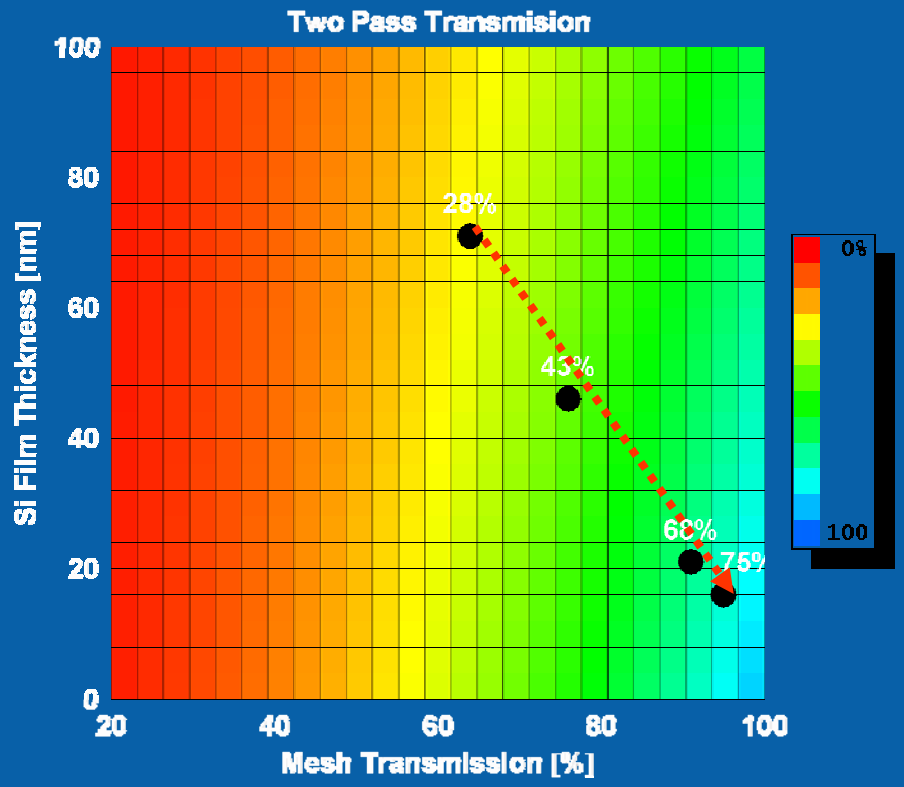
EUV Pellicle Concept (Choices are good!)



- Mesh apodizes the illuminator exit pupil and PO entrance pupil.
- Mesh film absorbs with both passes.

- The Concept
  - Thin film mounted on a wire-mesh
  - Mesh located “far” from reticle plane to defocus defects
  - Transmission requires a high percentage open area
  - Illumination uniformity requires partial coherence

Transmission Si With Ru Capping



Ru Capping Thickness = 2 nm per side

Innovation-Enabled Technology Pipeline

Technology Generation

90 nm
2003

65 nm
2005

45 nm
2007

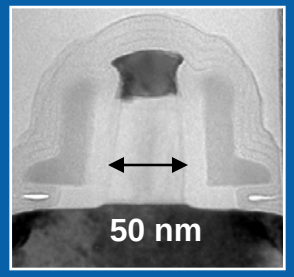
32 nm
2009

2011+

Manufacturing

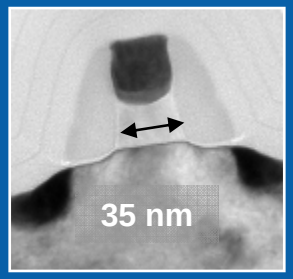
Development

Research



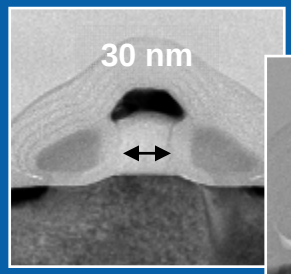
SiGe S/D

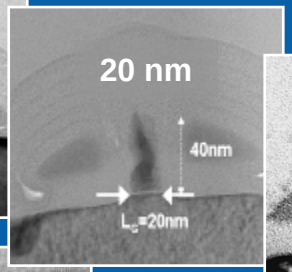
Strained Silicon

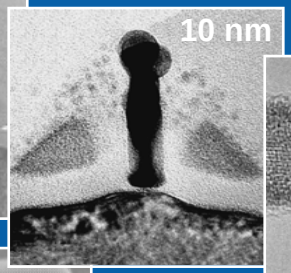


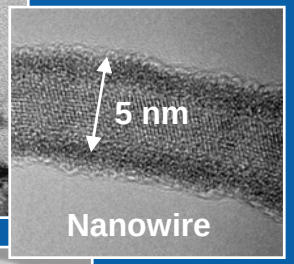
SiGe S/D

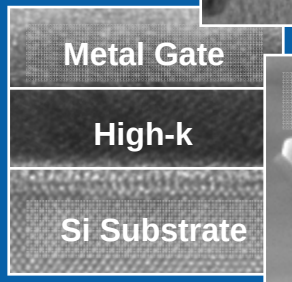
Strained Silicon

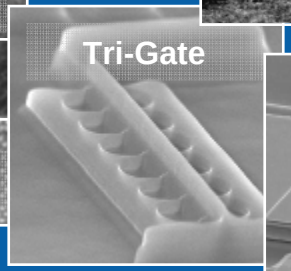


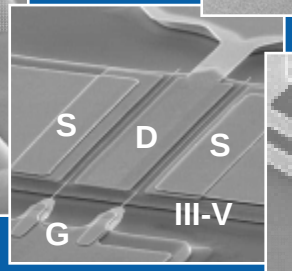












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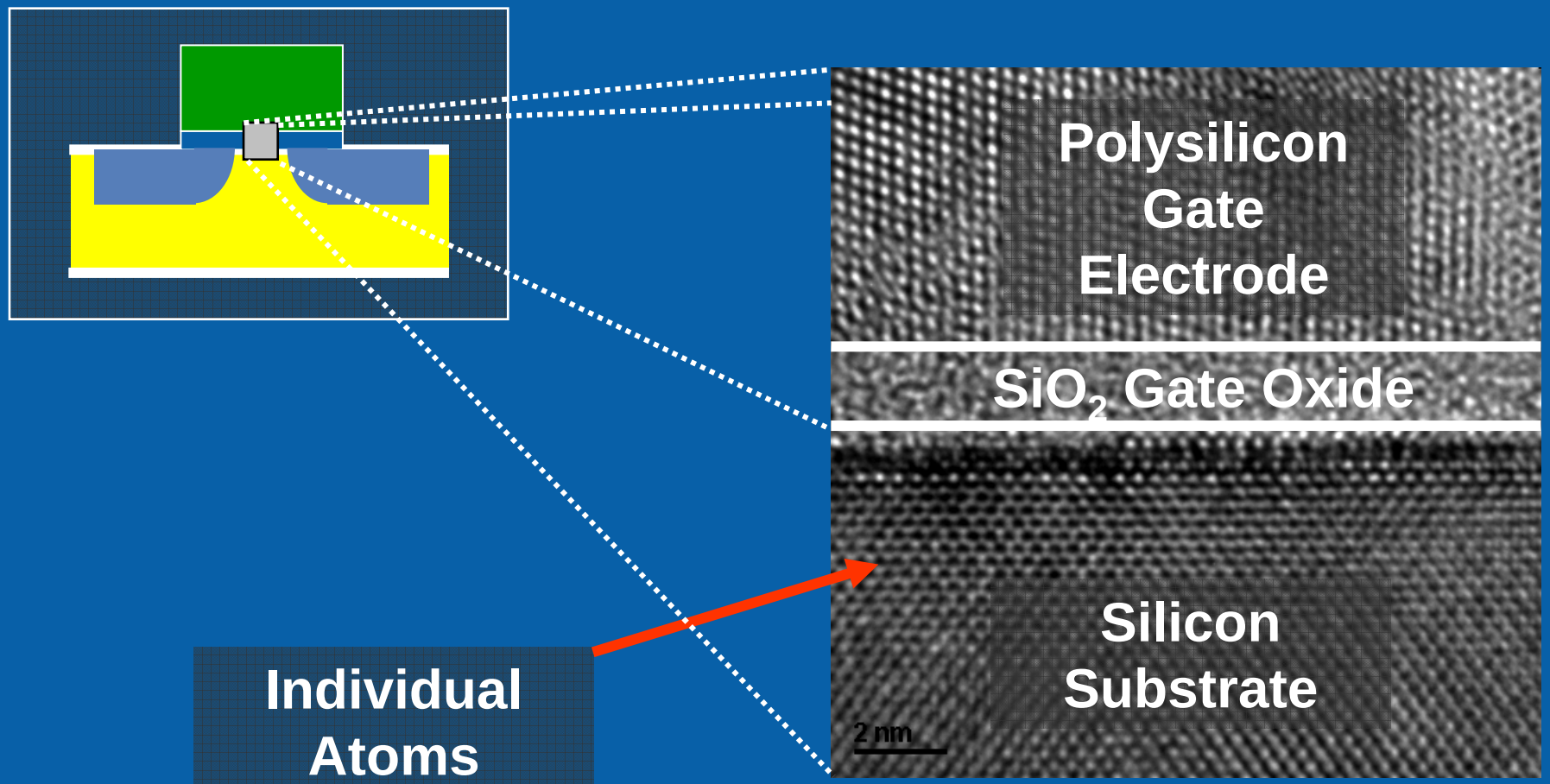
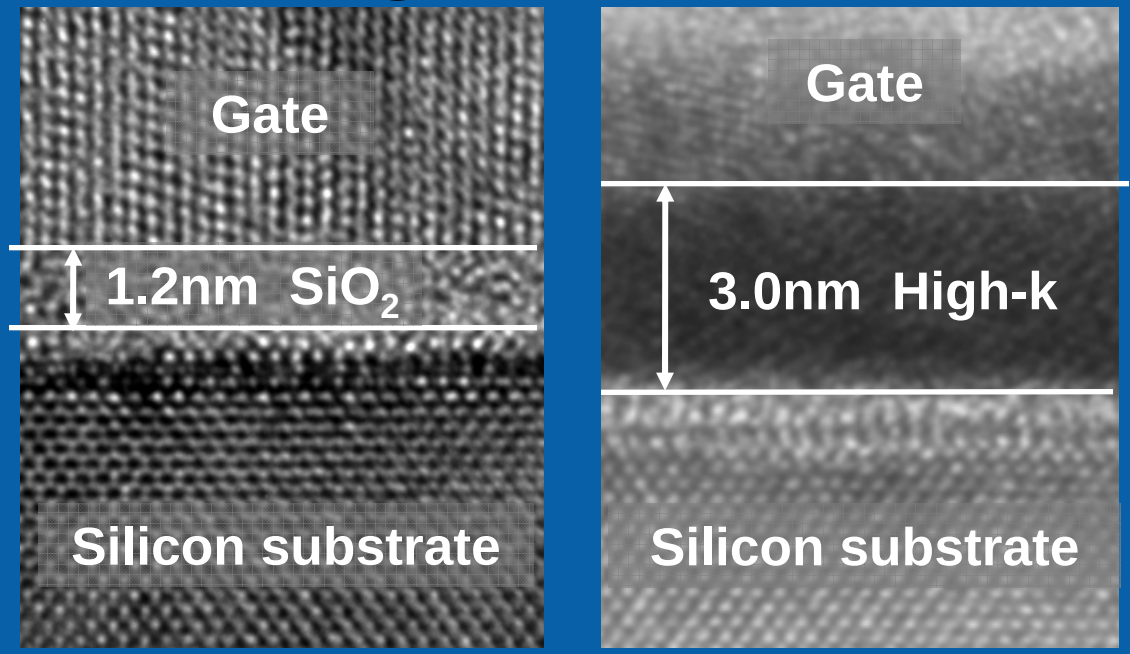
Future options subject to change

Source: Intel

Gate Dielectric Today is Only a Few Molecular Layers Thick



High-k Demonstrated >100x Leakage Reduction



Benefits compared to current process technologies

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*

Intel FUSI (Fully Silicided) Gate Transistors

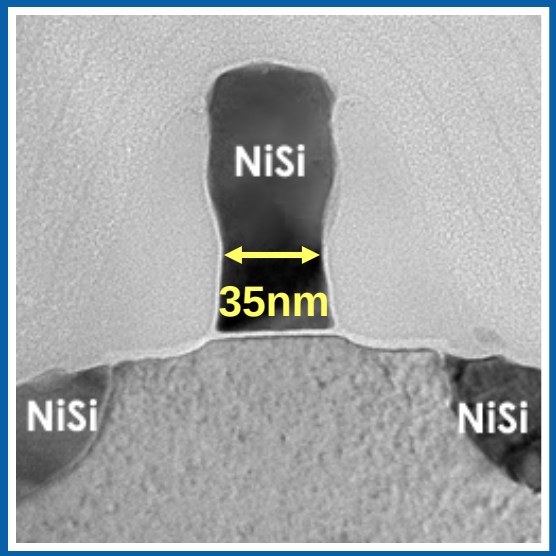
- Intel has successfully integrated FUSI (fully silicided) gates and uniaxial strained Si channels
- Performance gains from strained channels and FUSI gates fully additive
- Best transistor performance/leakage (I_{DSAT}-I_{OFF}) characteristics reported to date in industry
- Transistor performance, reliability and process integration have been thoroughly evaluated
- FUSI process can enable very high performance transistor technology for sub-65nm CMOS nodes

Transistor Performance Enhancement

Option for sub-65nm CMOS Technology

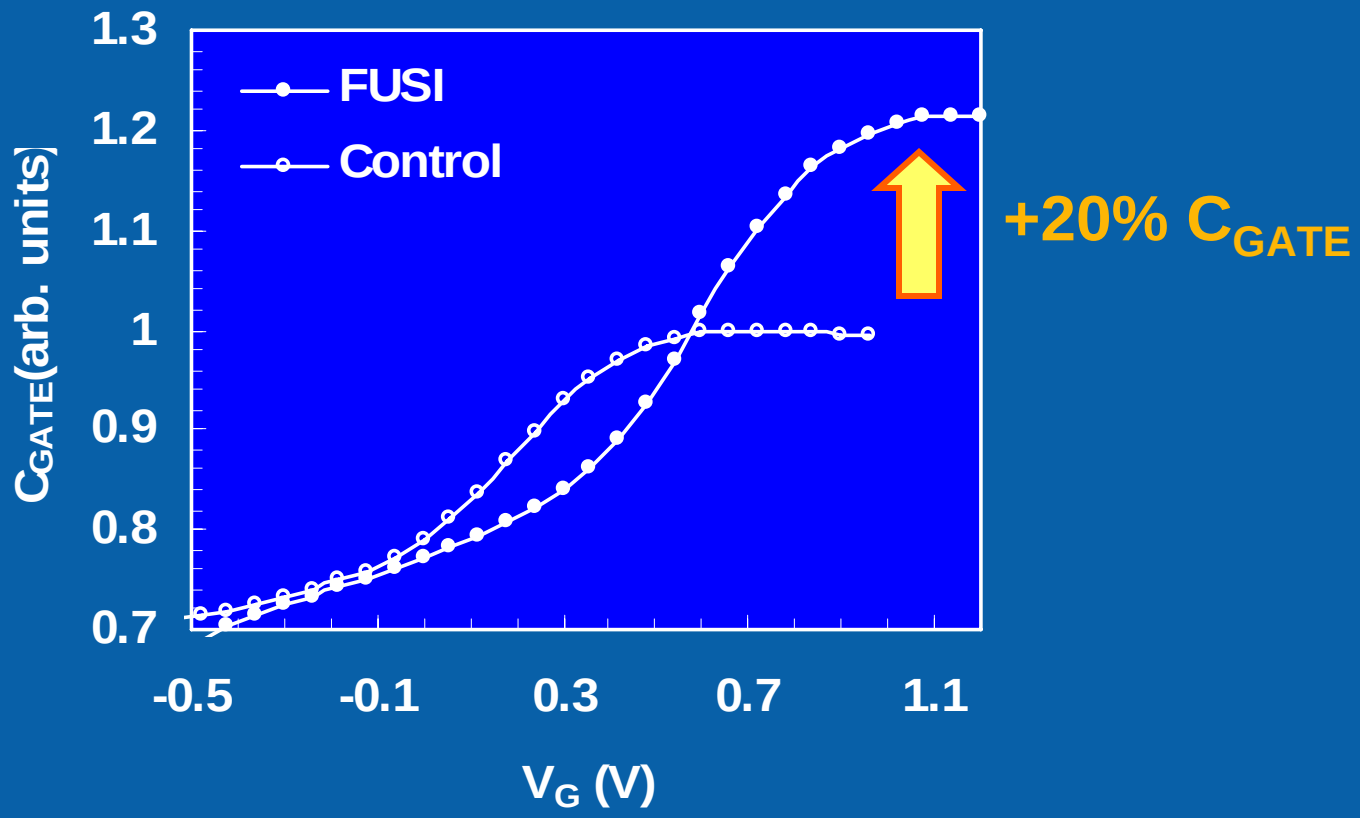
$$\textit{Transistor performance, } I_{DSAT} \propto \frac{W}{L} \cdot \mu \cdot C_{OX}$$

- Mobility Enhancement (μ)
  - Strained Si Channels
- Higher Gate Capacitance (C_{OX})
  - Hi-k dielectrics
  - Metal gate electrodes



FUSI: Gate Depletion Suppressed

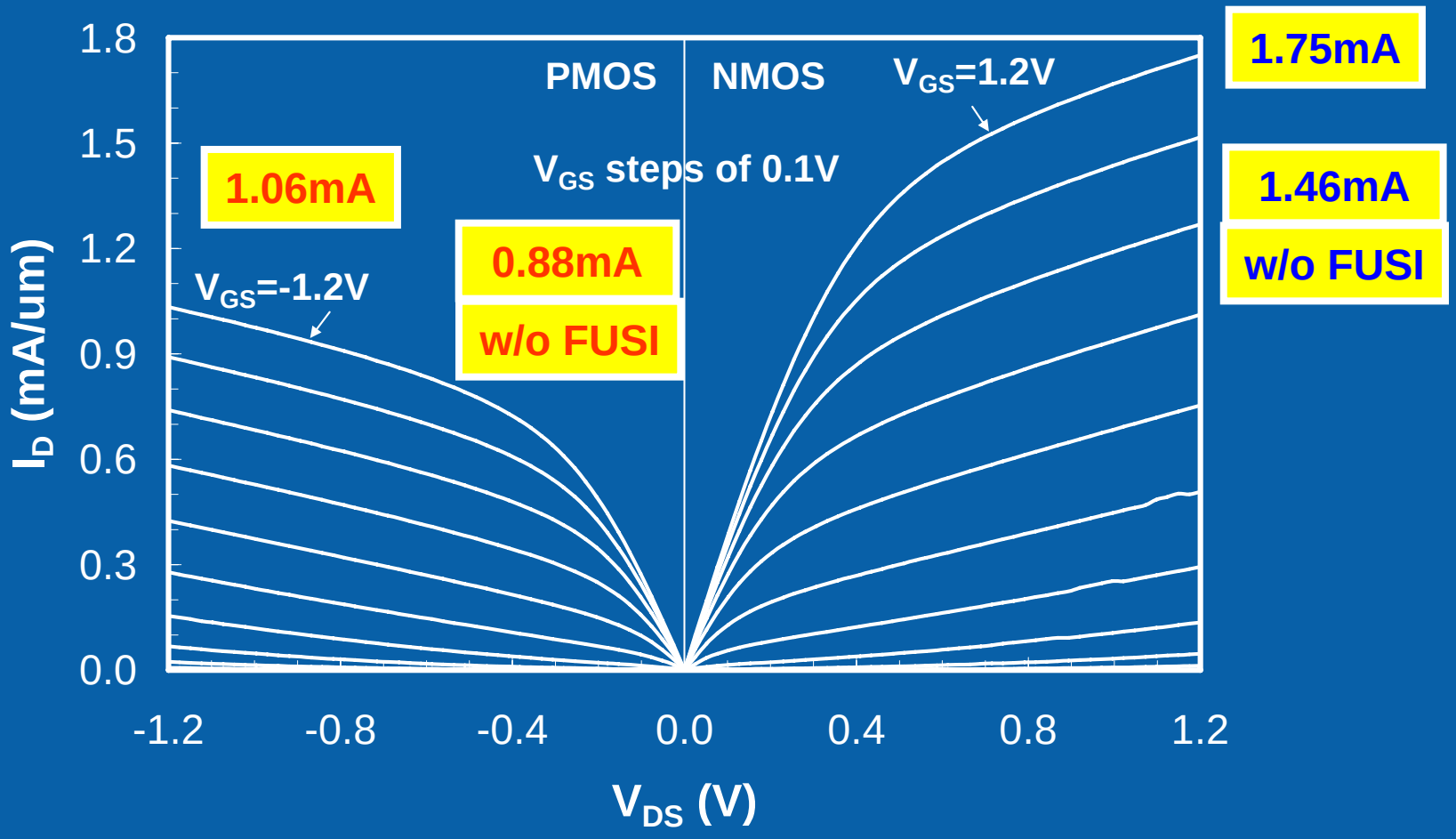
Enhancement in inversion charge density



- No gate depletion seen on FUSI devices
  - Higher C_{GATE} → Higher Q_{INV}
  - Higher Q_{INV} → Higher I_{DSAT}

FUSI Transistor Performance

I_D-V_D Characteristics



Healthy output characteristics for 35nm L_{GATE} devices

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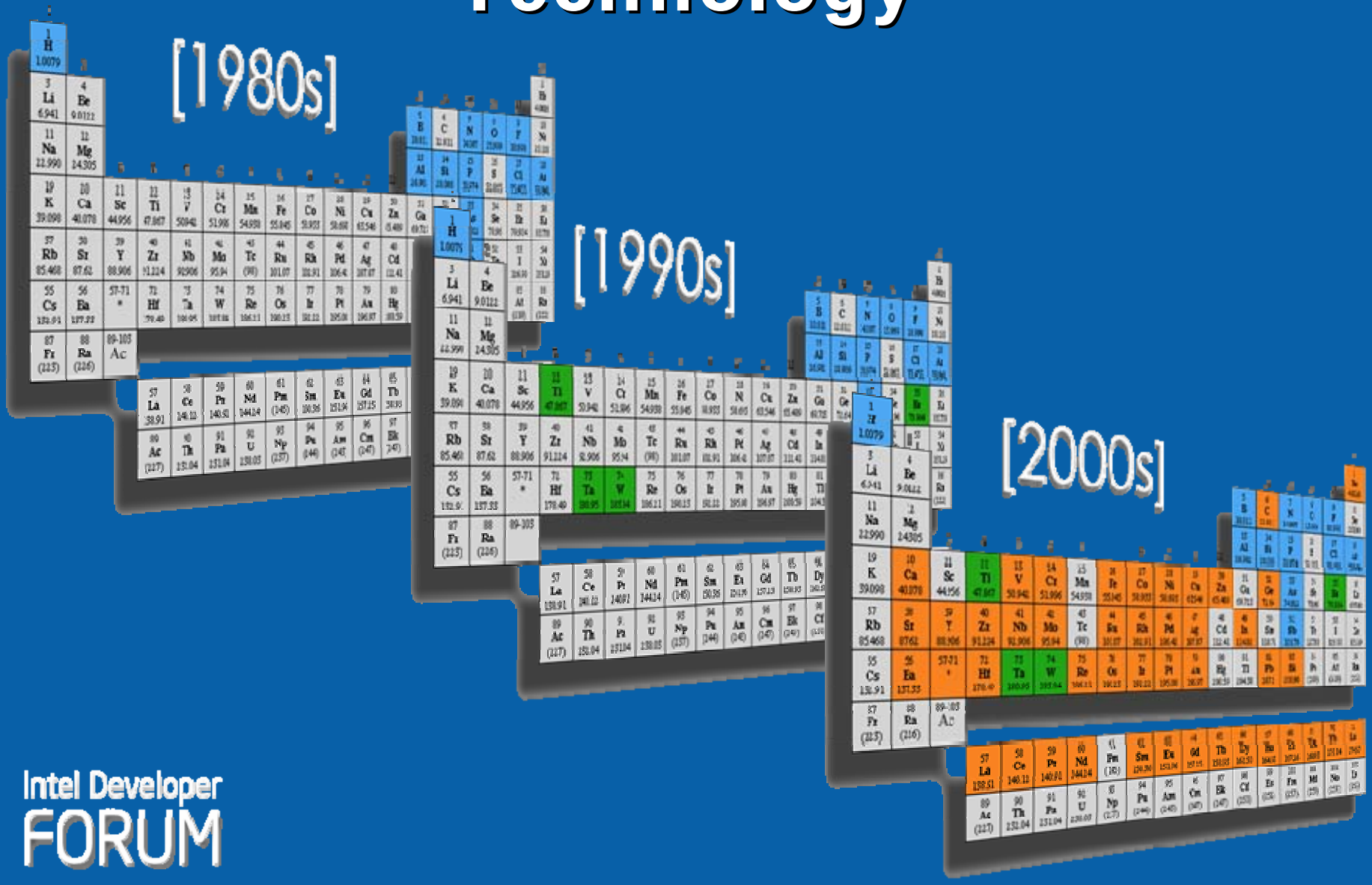
New Materials in Silicon Technology



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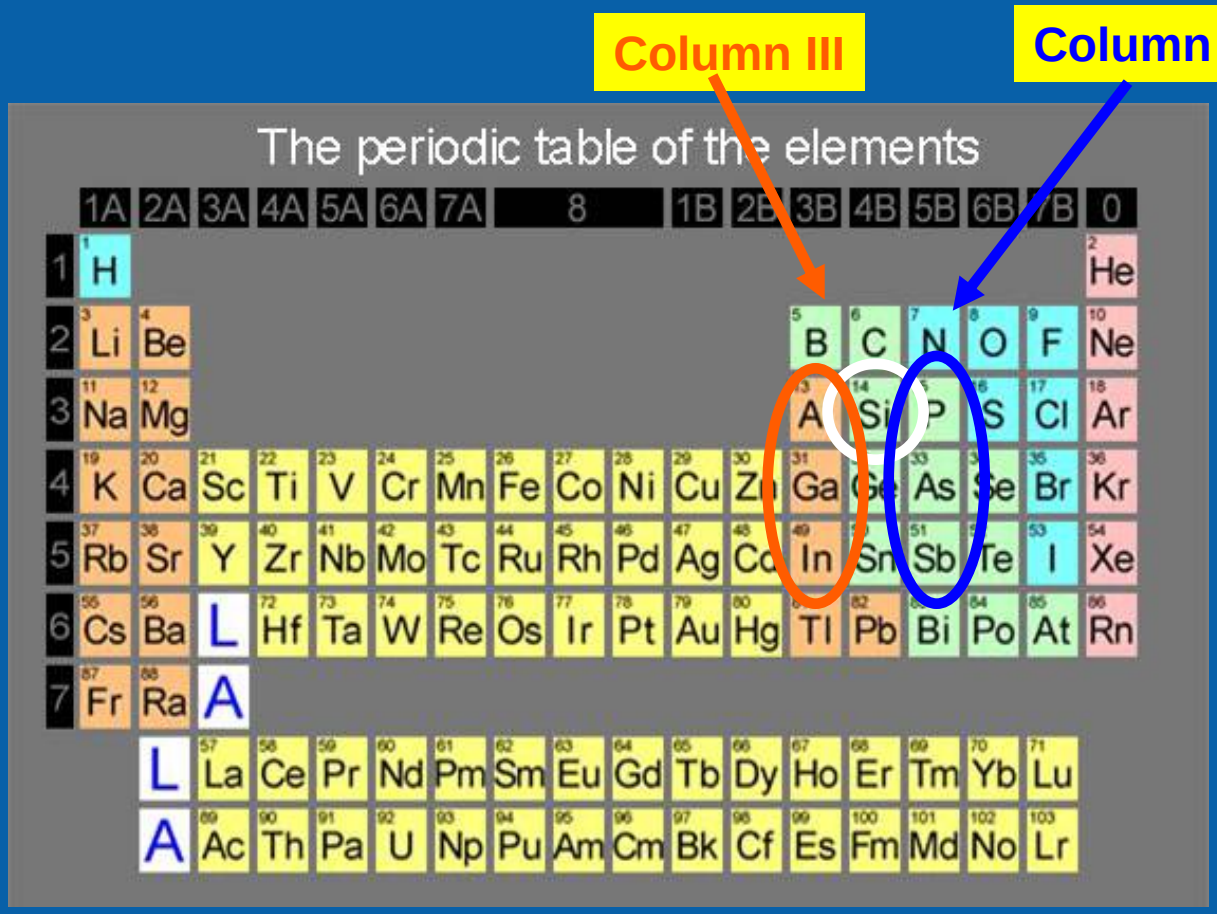
Compound Semiconductors



Si = Silicon
Al = Aluminum
Ga= Gallium
In = Indium
P = Phosphorous
As = Arsenic
Sb = Antimony

- Silicon in transistor channel is replaced by “III-V compound semiconductor”
- Result is much higher electron mobility, meaning significant performance and power improvements

Increasing Electron Mobility

Increased mobility in the transistor channel leads to higher performance and less energy consumption

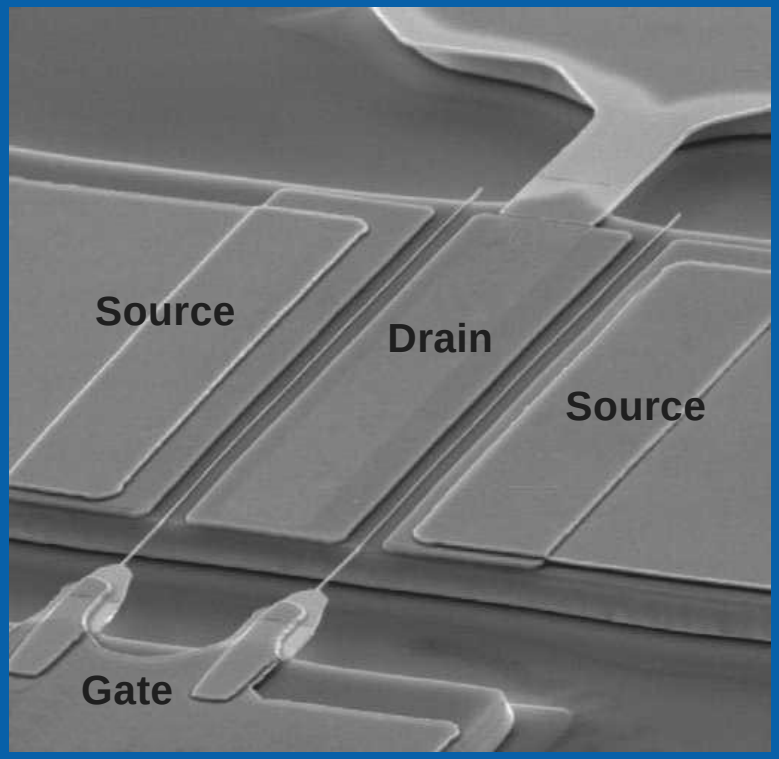
$$I_{DSAT} \propto \frac{W}{L} \cdot \mu \cdot C_{OX}$$

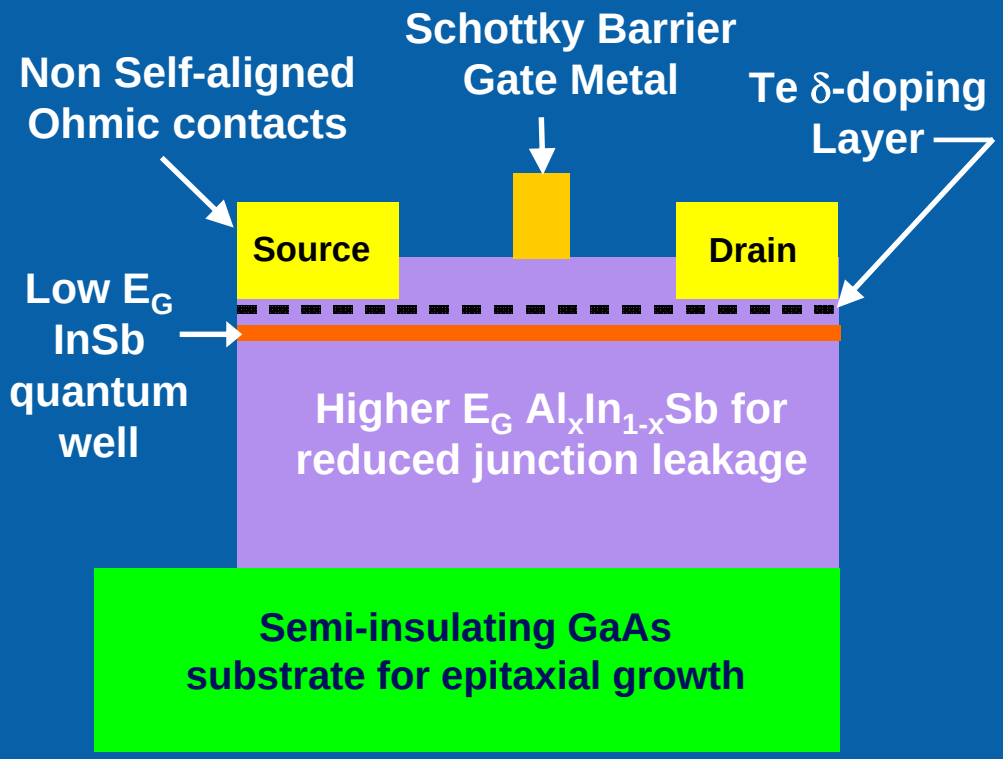
Relative mobility

	Compound Semiconductors		
Si	GaAs	InAs	InSb
1	8	33	50

Compound semiconductors have higher electron mobility than Si; InSb (indium antimonide) is highest of all

InSb QW* Transistor Fabrication





A two gate finger InSb QW transistor (QWFET*) is fabricated with gate air-bridge using mesa isolation

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*QW = Quantum Well

*FET = Field-effect Transistor

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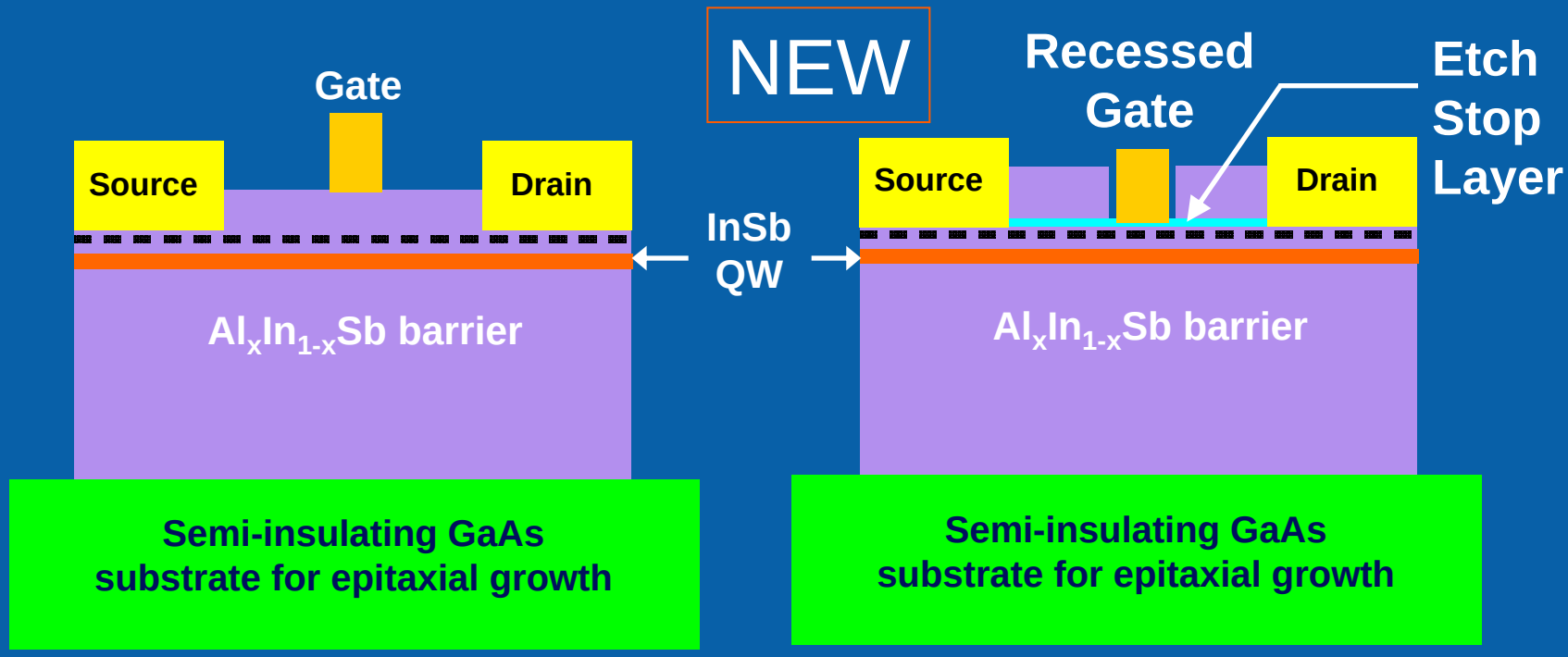
Depletion and Enhancement Mode



Depletion mode
(Normally ON)

Enhancement mode
(Normally OFF)

A novel gate recess process is used to fabricate enhancement mode InSb QWFETs

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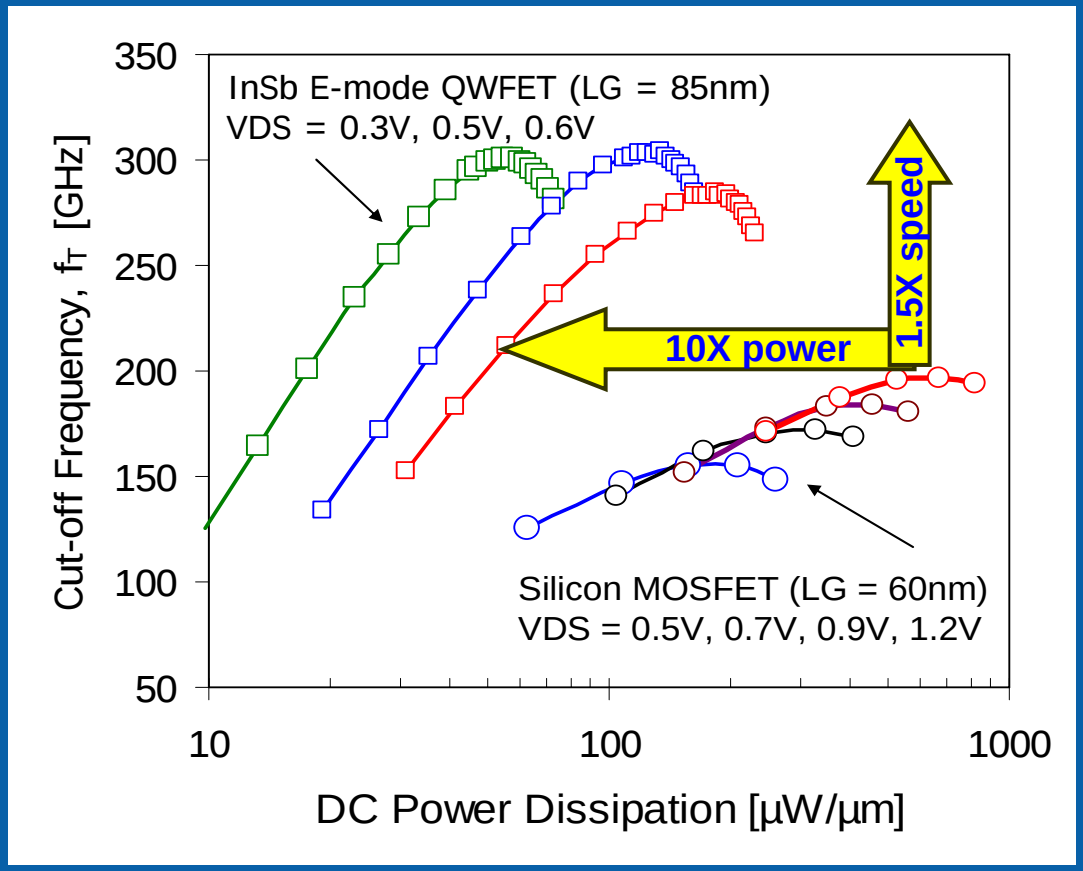
Speed, Power, Performance



InSb QWFETs show > 10x reduction in active power dissipation compared to Si MOSFETs

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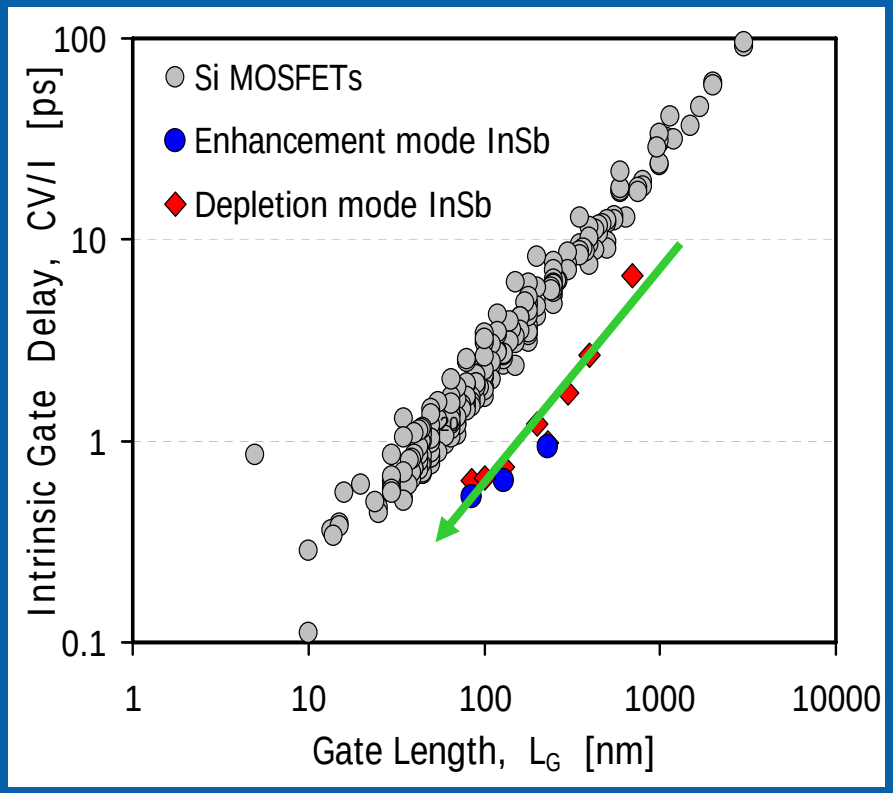
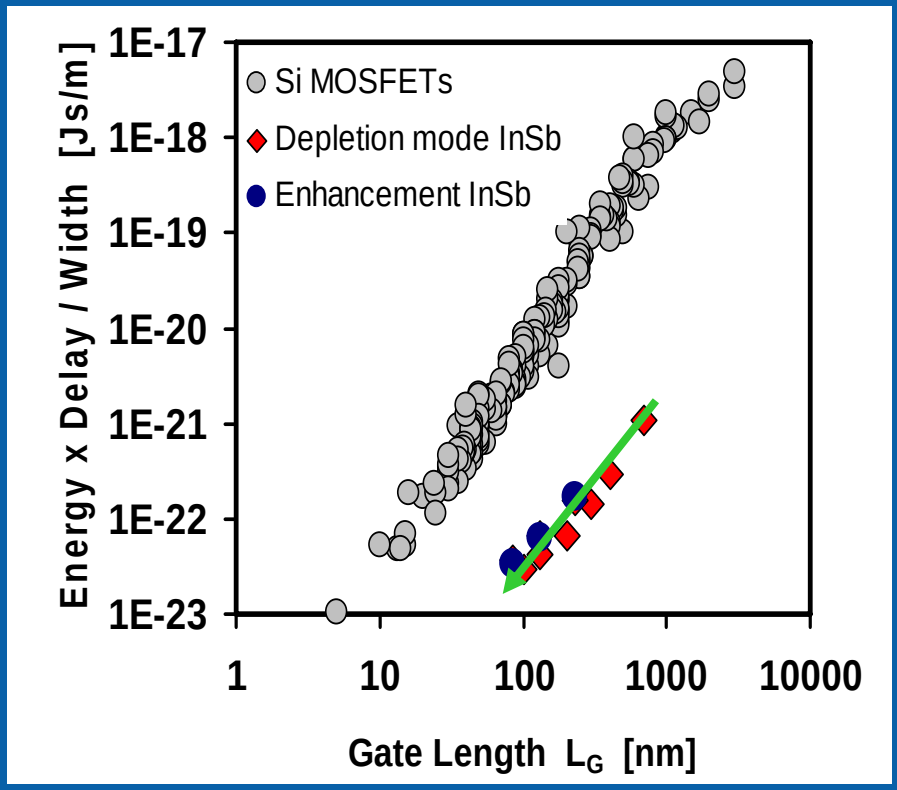
Benchmarking InSb QWFETs





InSb transistors show significant improvement in intrinsic gate delay and energy-delay product over Si MOSFETs at equivalent gate length

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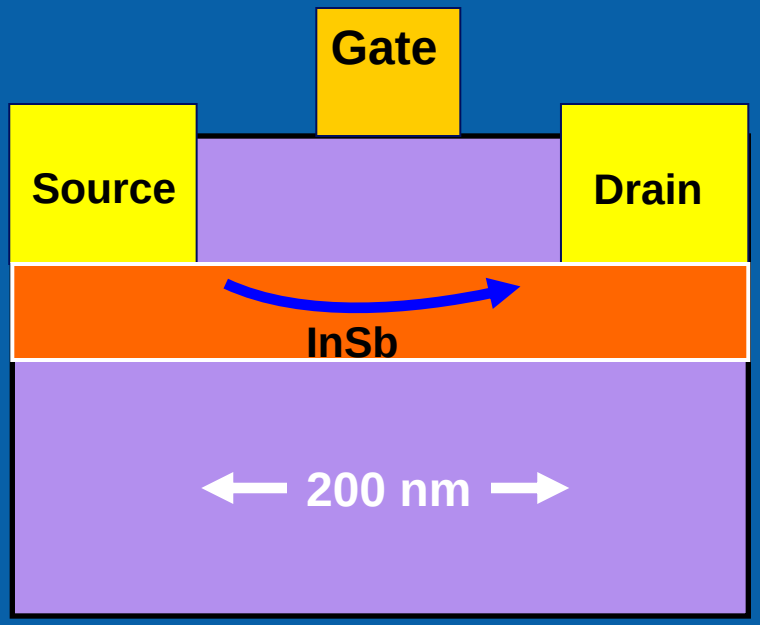
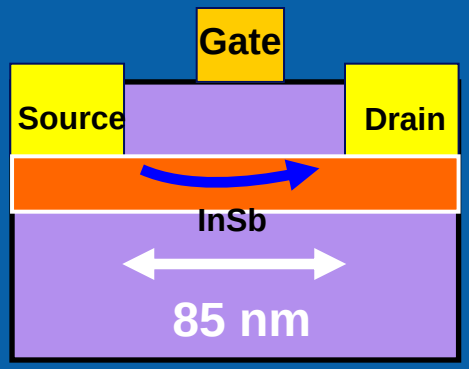
Research Improvements





Announced by Intel & QinetiQ, Feb. 2005

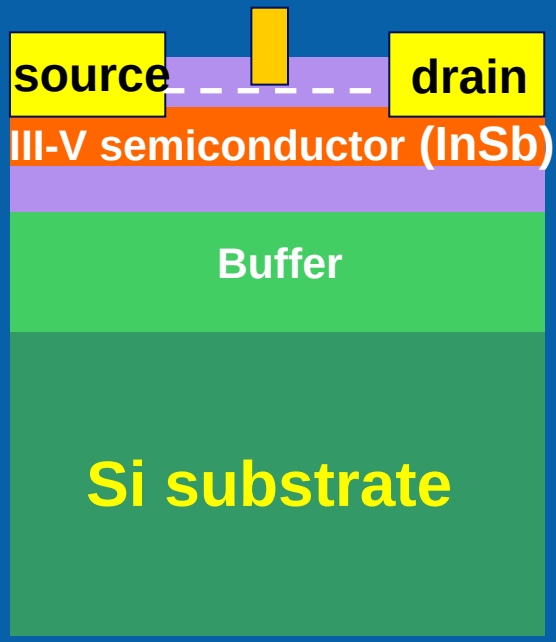
- InSb transistors for logic applications
- 200nm channel
- Depletion mode only (normally in 'on' state)

December 2005 announcement

- Channel length reduction to 85nm for higher speed
- Enhancement (normally in 'off' state) and depletion mode; both are required for logic circuits

	Si	InSb
Relative speed	1	50% higher
Relative active power	1	up to 10X lower

Integration on Si Platform



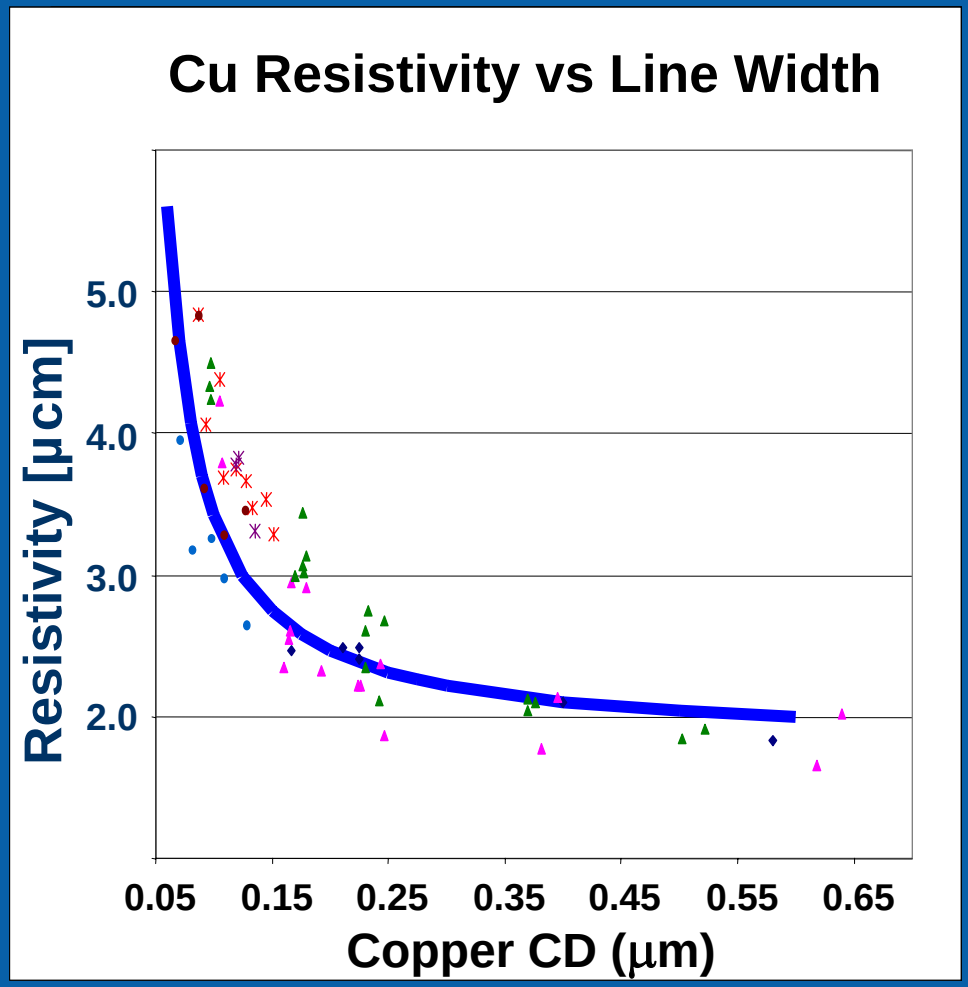
Current research on incorporation of new transistor onto the existing Si platform

Opportunities

- InSb QWFETs can potentially provide
  - 10X reduction in active power compared to Si MOSFETs from low V_{cc} operation
  - 50% higher intrinsic switching with speed at equivalent power
- Challenges include
  - III-V integration on Silicon substrate
  - Continued scaling to smaller dimensions

Metal Resistivity Scaling

- Resistivity is a growing concern as line widths scale down
- Effect of liner thickness and electron scattering doubles effective resistivity as metal width scales from 150nm to 75nm
  - Feature size is approaching mean free path of electrons in Cu



Source:Intel

Stacking Can Reduce Interconnect Lengths

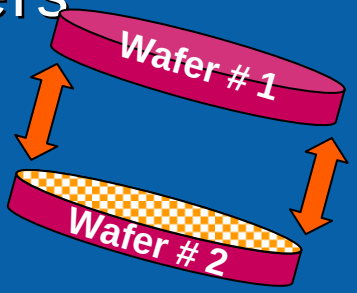
Basic Concept

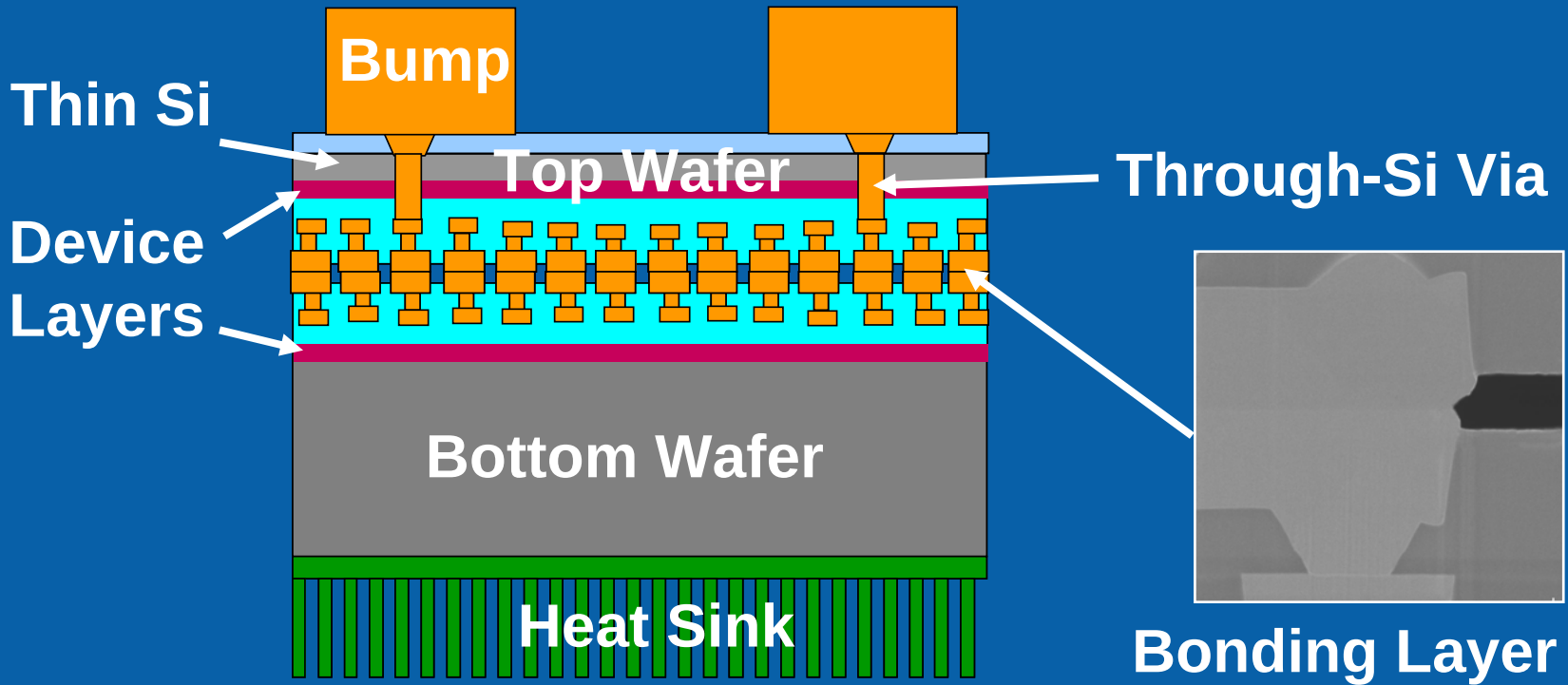
Stack layout reduces wire lengths

Reduces lengths between
1) logic to logic
2) logic to memory
3) Heterogeneous devices

3D Interconnects Research

- Cu bonding provides high-density low-resistance connections between device layers
- 300mm wafer-level stacking for fast throughput
- Through-Si Vias used for power and signal I/O

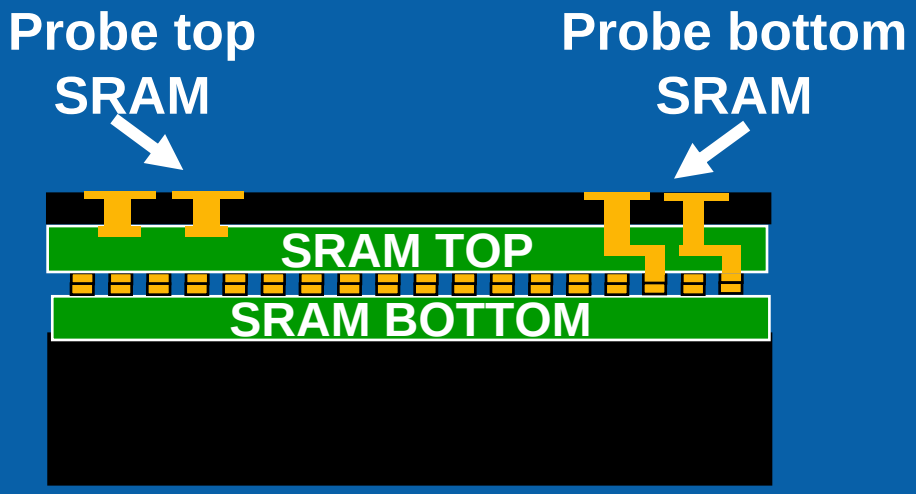


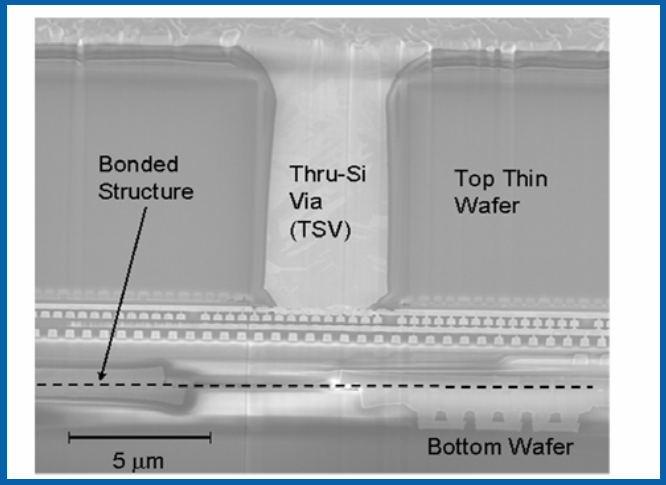


Bonding Layer (Cu)

Stacked SRAMs

- SRAMs in both top (in thin silicon) and bottom silicon were functional
- SRAMs were probed using the through-Si Vias; the bottom SRAM is probed through the bonding layer





Summary

- Only Intel has the process technology pipeline
  - Follows Moore's Law on 2-year-cycle
  - 65nm production Q4'05
  - 45nm prototype Q1'06
  - 65nm/90nm cross-over Q3'06
  - Tech options '07 and beyond
- Process tech is an important competitive advantage for Intel platforms
  - Industry-leading low-leakage transistors
  - In-house co-optimization
  - Holistic approach to world-class yield, energy-efficient performance, and leading-edge capacity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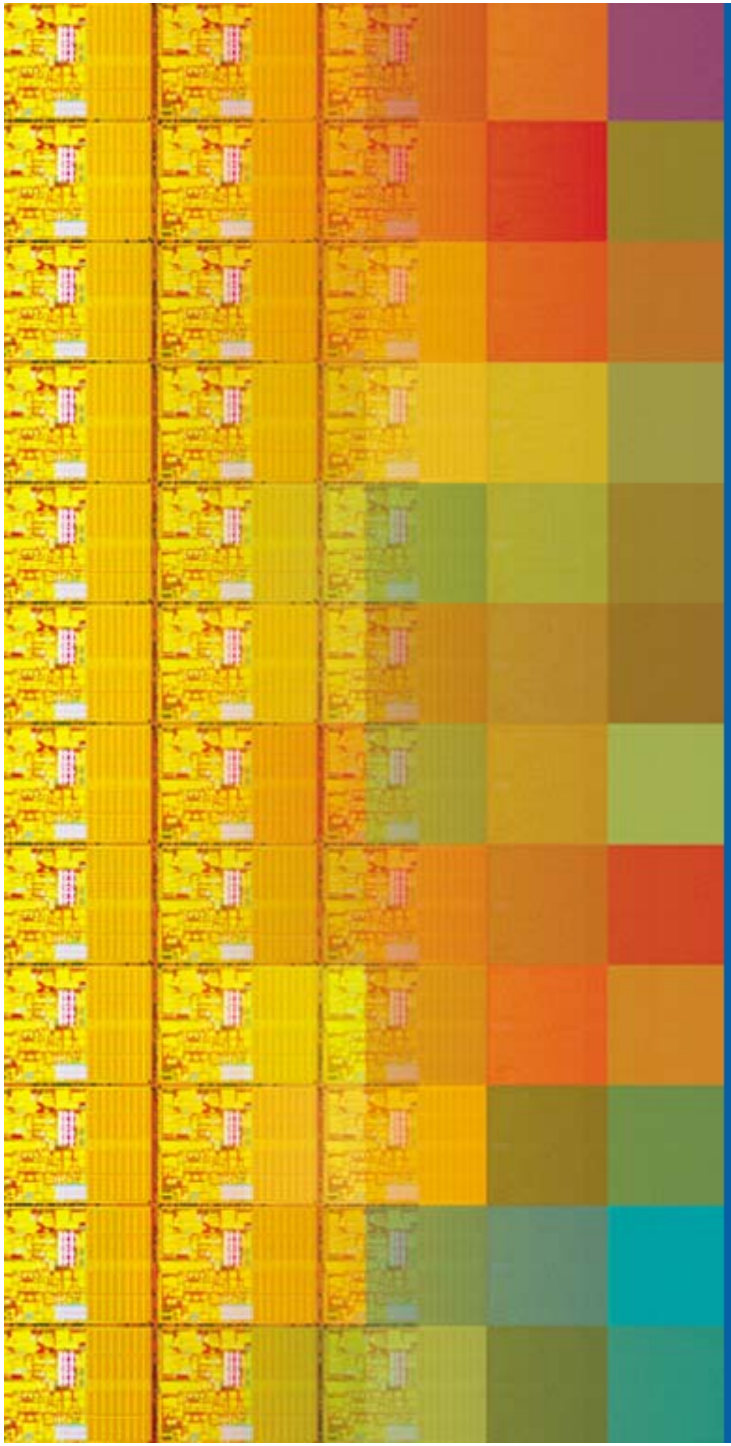

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Q&A

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